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Routing Power Reduction by Place and Route Algorithm on Different Architectures

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Abstract—**Shrinking area, higher density of logic blocks and ever increasing clock frequency calls for improvements and innovations in the field of circuit design. The increase in parameters like clock frequency and Configurable Logic Blocks (CLBs) are somehow directly related to the power consumption and on-chip temperature of the circuit. It is realized that much of the power dissipation happens in routing process and interconnection, hence this paper attempts to address this issue by running Placement and Routing algorithms on different switch-box (SB) architectures. During the Place and Route process, the circuit delays which are crucial in high speed circuits are also considered. These delays are optimally managed by the Place and Route algorithm. The simulations are carried out by running the standard MCNC benchmarks and the simulation results of routing, leakage, logical and total power consumptions are presented. Also the temperature spread-out across the FPGA is shown.**

Index Terms— **Interconnect power; Place and Route; Switch-Box Architecture; Temperature.**

I. INTRODUCTION

Low power design is perhaps one of the biggest challenges faced by designers today. The power consumed by an FPGA can be classified into static power consumption and dynamic power consumption. Static power is consumed by the device even when no input signals are exercised but dynamic power dissipation depend on the design parameters like clock frequency and utilization of CLBs. The static power consumption is usually critical for the device manufacturer and it depends on the physics and internal architecture of the device. The dynamic power consumption is important from the designer's point of view.

The overall power consumption is proportional to the product of frequency, supply voltage squared and capacitance [1]. Hence reduction in these parameters offers attractive techniques to reduce power consumption. A few techniques proposed are to dynamically scale the supply voltage depending upon the status of Input-Output buffers [2], using predictive shutdown of inactive components and recent techniques exploit the dynamic reprogrammablity to reduce power consumption [3].The placement and routing phases are particularly interesting class of problems as the designer has to follow the user constrains like net lists and also place and
route in such a way that wirelength, area, routing power and delay in critical paths are minimum. With the increasing popularity of machine learning techniques such as genetic algorithms and neural networks, these techniques have been adopted in circuit design to achieve the low power consumption goal. The genetic algorithms can be used for area optimization of the chip by Placement and Routing [4]. Another optimization technique is simulated annealing and it may be used for determining the placement of blocks such that interconnect wire lengths are minimized [5].

Most of the power consumption which is about 65% of total power dissipation in the device happen in routing process[6], and studies reveal that the power consumption of about 70% happen at the central portion of the device [7]. Now-a-days designers can build their own custom architecture depending on the purpose of utilization. Further the design is optimized for this architecture based on cost, performance or power consumption criteria. The Switch Box architecture is the way the horizontal blocks are connected to vertical blocks during routing in an FPGA. Most popular architectures are Wilton architecture, Subset Architecture and Universal architecture.

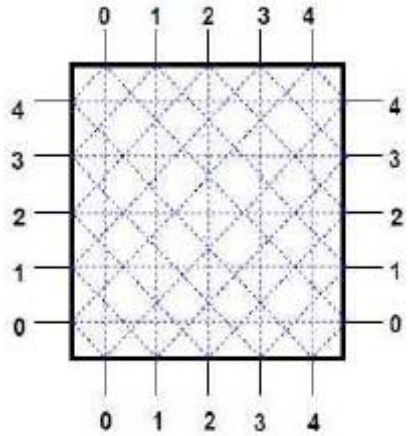

Fig.1. Universal architecture

This paper discusses the reduction of routing power by choosing the appropriate switch-box architecture and running Place and Route algorithm, considering the circuit delays and critical paths. The size of the Look-Up Table (LUT) is 4.

As the FPGA blocks are interconnected using wire segments, there exists capacitance. And the power dissipated as heat during charging and discharging of capacitance is a key issue. To address the temperature rise problem, auxiliary arrangements such as fans and heat sinks need to be included that increases the device area as well as the cost. The

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present research work addresses the temperature rise issue by Place and Route algorithm. The Placement and Routing is done in such a way that the device is maintained at ambient temperature.

II. Place and route methodology

After floor planning, the next thing is placement and routing. The placement and routing should be such that the utilization of the resources must be optimum. During the placement, care should be taken that the blocks should not be concentrated at a single region. Otherwise this will lead to rise in the temperature of that region. The placement and routing should be done taking consideration of wire lengths between the blocks. Fig.2. indicates the proposed methodology for Place and Route.

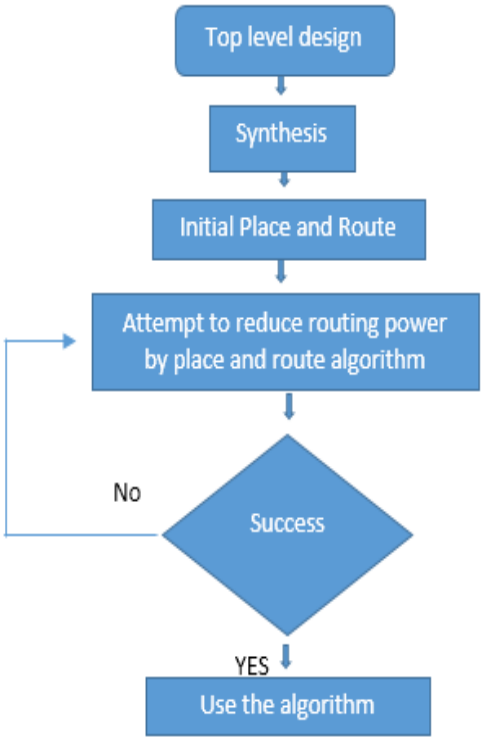
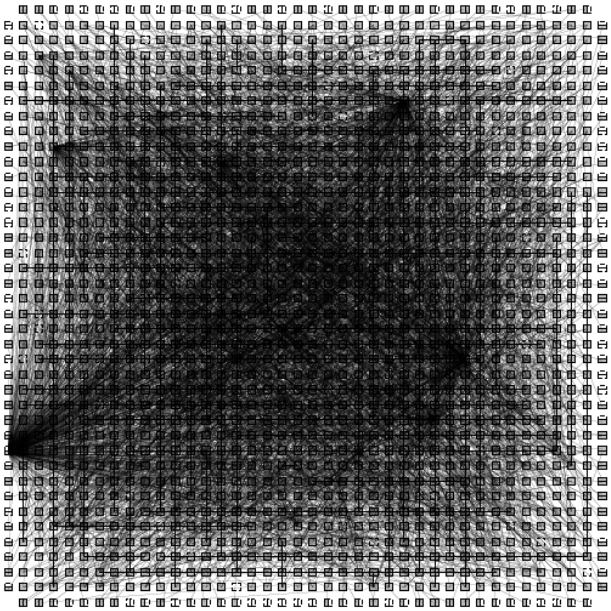
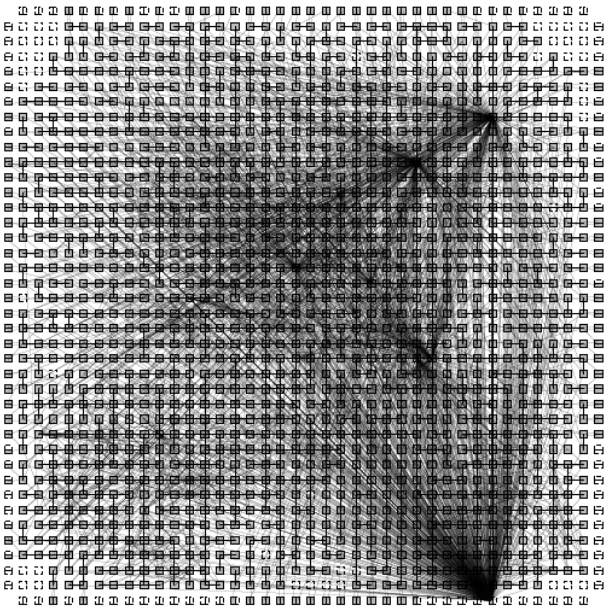


Fig.2.Proposed methodology for Place and Route

The mapping is done and considerable savings in wire length is observed. Also the density of the interconnections in routing is reduced which takes care of temperature rise problems. The satisfactory improvements in delay and overall implementation costs are reduced. The mapping plots Fig.3. are obtained on an MCNC standard design benchmark called as *tseng*.



(a)



(b)

Fig.3. (a) Initial Mapping and (b) Final Mapping

III. The routing power

As mentioned earlier, the routing power constitutes nearly 65% of total power dissipation. The routing power is the power dissipated in the interconnections and is highly dependent on the placement and routing architecture. An optimum routing is one where the routing power is distributed across the device uniformly. But this sometimes comes with the price of increase in wirelength between the interconnections. To reduce the routing power the wirelength as well as optimum utilization of resources is necessary. The place and route algorithm is run for two architectures, namely custom architecture and universal architecture on an MCNC design benchmark called *misex3* and simulation results are shown in Fig.4. It is observed that the interconnection power for universal architecture is spread across the device and the power dissipation at certain

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regions is decreased, avoiding the temperature rise problem.

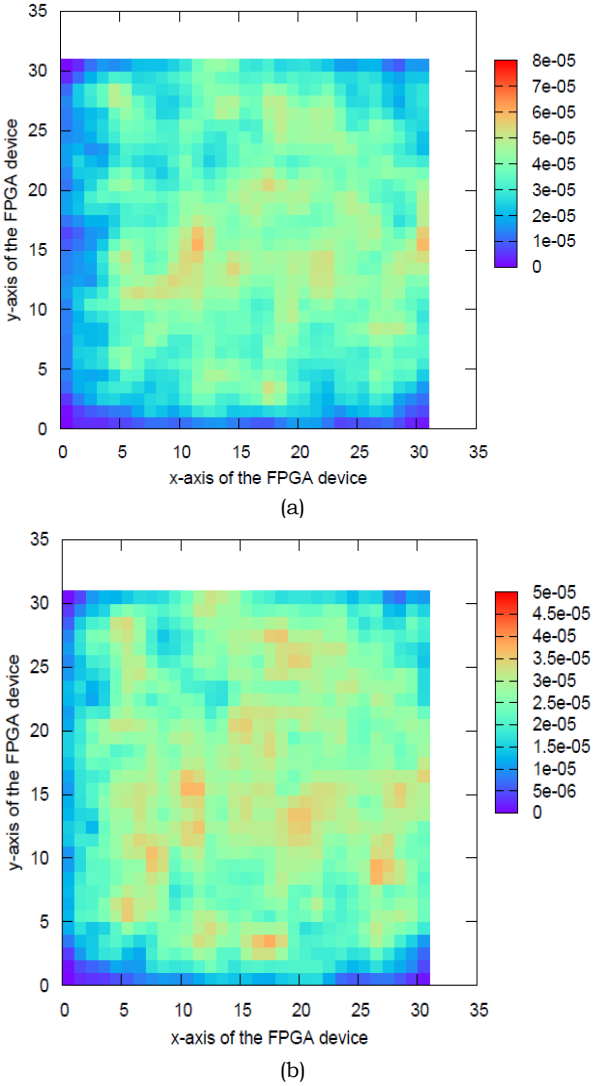

Fig.4. Interconnection power dissipation for (a) Custom Architecture and (b) Universal Architecture

IV. Temperature constraints

The power dissipation usually happens in the form of heat. This may rise the temperature of the device which will affect the performance and reliability of the device. Hence it is necessary to maintain the device at ambient temperature. The temperature of operation can be controlled by optimum placement and routing. Two very active blocks must not be placed side by side; otherwise will create a region whose temperature will increase beyond the specified range. In routing, if the interconnections have high density, the power is dissipated as heat. This is due to the fact that, there will be capacitance formed between the two wire segments that will constantly charge and discharge. In the Place and Route algorithm used in this paper, attempts to distribute the temperature across the device uniformly. The ambient operating temperature for the device is taken to be 28 degree Celsius and the Place and Route algorithm is run for custom architecture and universal architecture on an MCNC design benchmark called *alu4* and the temperature distribution across the device is plotted for universal architecture on a normalized scale. It is observed that there is not much difference in terms of temperature distribution in both the architectures. Fig.5. gives the temperature distribution for Custom architecture.

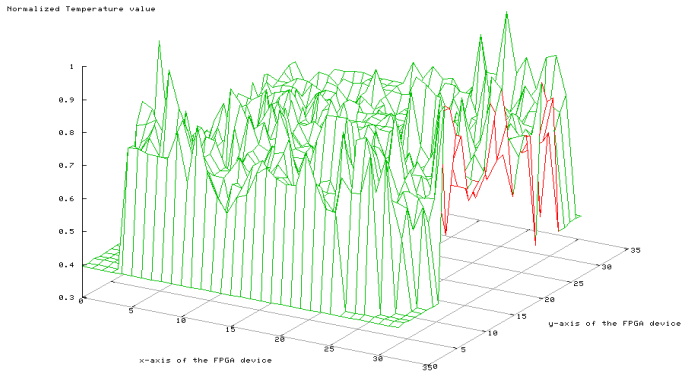

Fig.5. Temperature distribution for Custom Architecture

V. Simulation Results

The different MCNC benchmarks used for testing and the number of CLBs used is listed in Table I. The various power dissipations namely routing power, logical power along with the total power dissipation for the custom and universal architectures using different benchmarks for testing is indicated in Table II.

TABLE I
Utilization chart of CLBs for different benchmarks

Benchmarks	Number of Inputs	Number of Outputs	CLBs Used
alu4	14	08	973
bigkey	229	197	1710
ex5p	08	63	642
fft_256	03	12	96
misex3	14	14	956
tseng	52	122	1401

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TABLE II Simulation results for various benchmarks and corresponding power dissipations

Benchmark	Architecture						Percentage Power Saving
	Custom			Universal			Custom/Universal
	Routing Power (W)	Logical Power (W)	Total Power (W_C)	Routing Power (W)	Logical Power (W)	Total Power (W_U)	$\{(W_U - W_C)/W_U\}*100$ + for Custom, -for Universal
alu4	0.0270827	0.00374825	0.0413939	0.0322509	0.0044407	0.049798	16.87(Custom)
bigkey	0.0643812	0.0115838	0.102893	0.0599577	0.011249	0.097221	-5.83(Universal)
ex5p	0.0230432	0.00255492	0.02556	0.019728	0.0022358	0.0279	8.38(Custom)
fft_256	0.0035618	0.00113135	0.0071126	0.0038245	0.0011329	0.007380	3.63(Custom)
misex3	0.040487	0.0051801	0.0543726	0.0293054	0.0039479	0.039477	-37.73(Universal)
tseng	0.0393388	0.00949625	0.0675254	0.0361347	0.0088966	0.062367	-8.27(Universal)

From the simulation results it is observed that a power saving of 16.87% is achieved in case of custom architecture for the *alu4* benchmark while the power consumption increases by 5.83% for the same architecture with benchmark *bigkey*

VI. Conclusion

The simulation results confirm that the routing power dominates overall power consumption. Selection of particular switch box architecture affects the power consumption. Hence it may be concluded that, for least power consumption an optimum architecture has to be chosen depending on the utilization purpose.

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