

Implementation of Second Generation Current Conveyor and its applications

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Abstract— In this paper simple CMOS second generation positive and negative current conveyors, CCII+ and CCII- are presented, suitable for low supply voltage operation. Operation of these Class AB circuits has been verified through Electric VLSI design system and LTspice simulations based on 32nm CMOS technology parameters at supply voltage of ±0.9V. Simulation results demonstrate the use of the CCII+ and CCII- in voltage differentiator applications. Voltage mode all pass filters are implemented using CCII-.

Index Terms— CMOS, Current mode, Current Conveyor

I. INTRODUCTION

The dominating motivation in analog integrated circuits design is small size, low-voltage and low-power design to be effective for portable systems, where the main voltage supply is a single or multi-cell battery that must maintain for long time. In this area, traditional voltage-mode techniques are being substituted by the current-mode approach, as the latter architectures are able to overcome the limitation of a constant gain-bandwidth product than the voltage mode type. So the current mode circuit's performance is improved in terms of low-voltage characteristics, slew rate and bandwidth [1].

The basic current-mode building block can be considered as Current Conveyor (CC), which uses an Op-Amp like approach in voltage mode circuits. Sedra and Smith introduced the current conveyors in 1968 [2] but the current conveyor success came only when second generation current conveyor (CCII) was introduced, in 1970 [3].

II.TOWARDS THE CMOS CCII REALIZATION.

The CCII is a three terminal device as shown in Fig. 1.

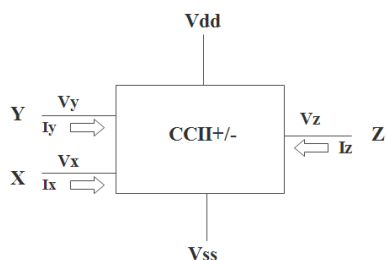


Fig.1. Basic CCII block diagram

Any voltage that appears at the X terminal also appears at the Y terminal and that any current that flows out of the Y terminal also flows out of the Z terminal,[4][5] where in

Positive second generation current conveyor (CCII+)

$$I_z = +(I_y). \quad (1)$$

And Negative second generation current conveyor (CCII-)

$$I_z = -(I_y). \quad (2)$$

A.CMOS CCII+ CIRCUIT DESCRIPTION & OPERATION.

Fig. 2 shows the transistor schematic for the CMOS Positive second generation current conveyor (CCII+) that was designed in [5] using 32nm CMOS parameters provided by [6]. Transistors M1 and M3 are designed with the same dimensions, the same dc bias current flows through them ($I_{d1} = I_{d3}$), and the same dc drain source voltage (the same applies for M2 and M4, respectively).

$$\frac{W1}{L1} = \frac{W3}{L3} = n \quad (3)$$

$$\frac{W2}{L2} = \frac{W4}{L4} = n1 \quad (4)$$

Therefore, any change in the voltage at X will produce a change in current in M1 and thus the same change in current in M3, which in turn produces the same voltage at Y that is at X. Transistors M5 and M7 are designed so that the same current that flows in M5 and M3 and out of Y terminal also flows in M7 and out of the Z terminal. [5]

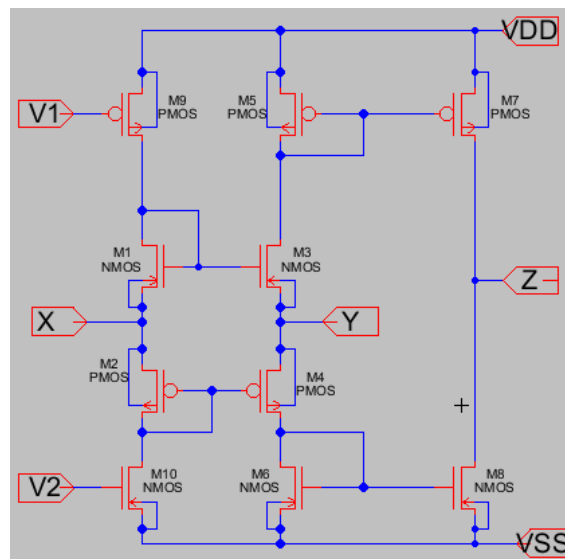


Fig.2. Positive second generation current conveyor (CCII+)

B. CMOS CCII- CIRCUIT DESCRIPTION & OPERATION.

Fig. 3 shows the transistor schematic for the CMOS Negative second generation current conveyor that was designed in [7] using 32nm CMOS parameters provided by [6]. Transistors M1 and M2 are designed with the same dimensions, the same dc bias current flows through them ($I_{d1} = I_{d2}$), and the same dc drain source voltage (the same comment applies for M3 and M4, respectively).

$$\frac{W1}{L1} = \frac{W2}{L2} = n \tag{5}$$

$$\frac{W3}{L3} = \frac{W4}{L4} = n1 \tag{6}$$

This means that any change in the voltage at X will produce a change in current in M1 and thus the same change in current in M2, which in turn produces the same voltage at Y that is at X. M7 is designed so that the same current that flows in M2 and out of Y terminal also flows in M5 and out Z terminal. (again, this is true for M2, M5 is also true for M4, M6 respectively)[7][8][9].

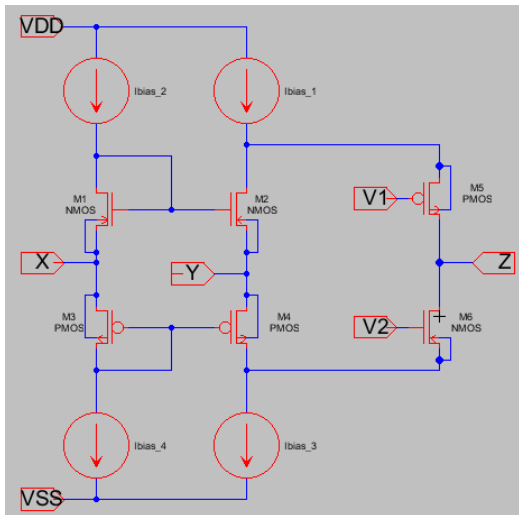


Fig.3. Negative second generation current conveyor (CCII-)

III. SIMULATION RESULTS

CCII+ & CCII- were simulated using the 32nm CMOS parameters. The Transistor aspect ratios used are given in table 1 & 2. The current transfer characteristics and voltage transfer characteristics of CCII+ and CCII- obtained are shown below in fig. 4,5,6,7. The supply voltages used for the proposed CCII are ± 0.9 V.

All the schematics are drawn in Electric VLSI Design Systems [11] and the simulations are obtained using LTspice [12].

Table 1: Transistor aspect ratios for Positive second generation current conveyor (CCII+)

Transistor	Type	Width(nm)	Length(nm)
M1	NMOS	1462	148
M2	PMOS	2590	157
M3	NMOS	1462	148
M4	PMOS	2590	157
M5	PMOS	9176	268
M6	NMOS	8110	222
M7	PMOS	9176	268
M8	NMOS	8110	222
M9	PMOS	2590	65
M10	NMOS	1295	259

All transistors operate in their saturation regions.

Table 2: Transistor aspect ratios for Negative second generation current conveyor (CCII-)

Transistor	Type	Width(nm)	Length(nm)
M1	NMOS	1302	65
M2	NMOS	1302	65
M3	PMOS	2604	65
M4	PMOS	2604	65
M5	PMOS	2604	260
M6	NMOS	521	260

All transistors operate in their saturation regions.

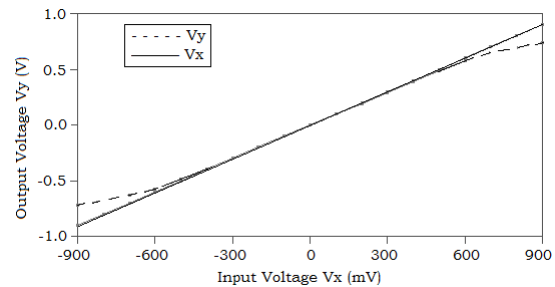


Fig.4. Positive second generation current conveyor (CCII+) as Voltage Follower

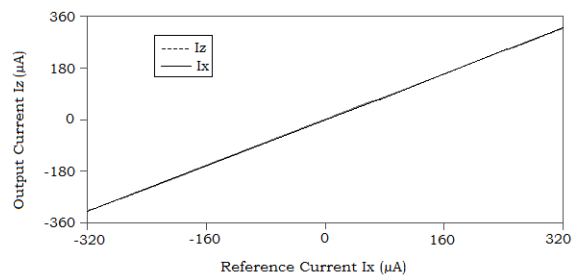


Fig.5. Positive second generation current conveyor (CCII+) as Current Follower

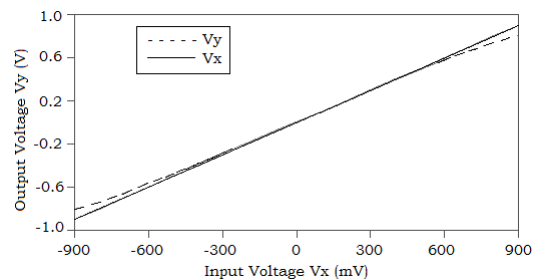


Fig.6. Negative second generation current conveyor (CCII-) as Voltage Follower

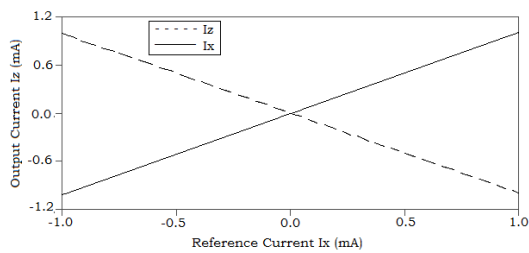


Fig.7. Negative second generation current conveyor (CCII-) as Current Follower

IV. APPLICATIONS BASED ON CCII+ AND CCII-

Current conveyors are very powerful building blocks, allowing analog designers to implement configurations with performance that are similar or, in some cases, improved with respect to their opamp based counterparts [1].

A. VOLTAGE DIFFERENTIATOR BASED ON CCII+

Voltage differentiator using two blocks of CCII+ and 2 passive elements is given below [1].

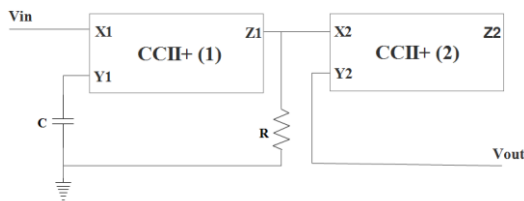


Fig.8. CCII+ based Voltage differentiator

Behavior of the circuit is explained by the output voltage expression:

$$V_{out} = V_{x2} = V_{y2} = R I_{z1} = R I_{x1} = sRCV_{x1} = sRCV_{y1} = sRCV_{in} \quad (7)$$

The voltage differentiator is simulated using LTspice with 32nm CMOS parameters. The Circuit operates at 0.6V, R=10kΩ and C=10μF.

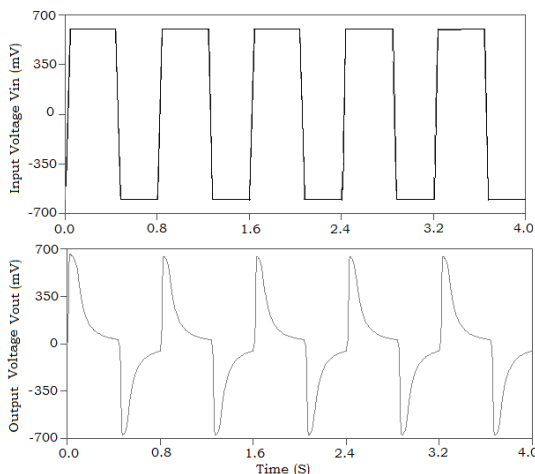


Fig.9. CCII+ based Voltage differentiator response to pulse input

B. VOLTAGE DIFFERENTIATOR BASED ON CCII-

CCII- based voltage differentiator is a non-inverting configuration. Traditional inverting configurations can be implemented simply changing the type of CCII. Voltage differentiator using two blocks of CCII- and 2 passive elements is given below [1].

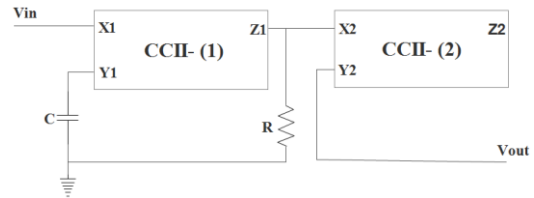


Fig.10. CCII- based Voltage differentiator

The voltage differentiator is simulated using LTspice with 32nm CMOS parameters. The Circuit operates at 0.9V, R=10kΩ and C=0.01μF.

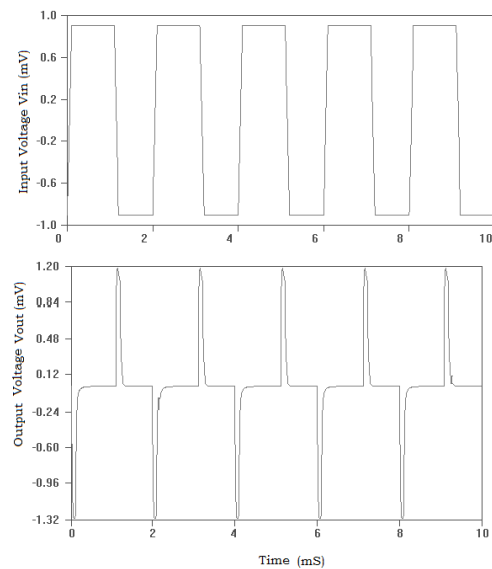


Fig.11. CCII- based Voltage differentiator response to pulse input

C. VOLTAGE MODE ALL PASS FILTER USING CCII-

Two novel networks for realizing all-pass filter with high input impedance using a single CCII and four passive elements.

The networks in Figs. 11 (a) and (b) depict a phase shift from 0° to -180° from +180° to 0° without constant loss in an all-pass characteristic, respectively. [10]

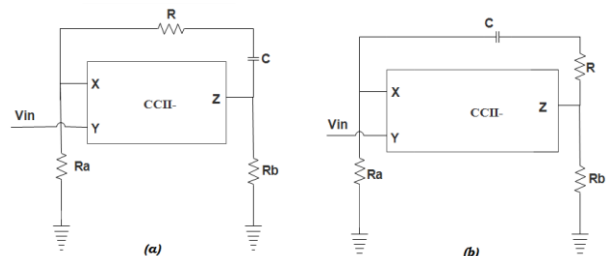


Fig.12. CCII- based Voltage mode all pass filter

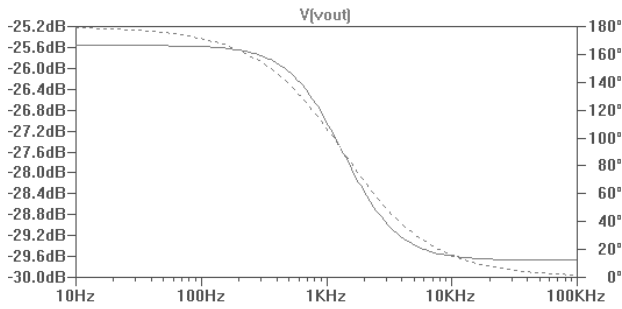


Fig.13.CCII- based Voltage mode all pass filter frequency response

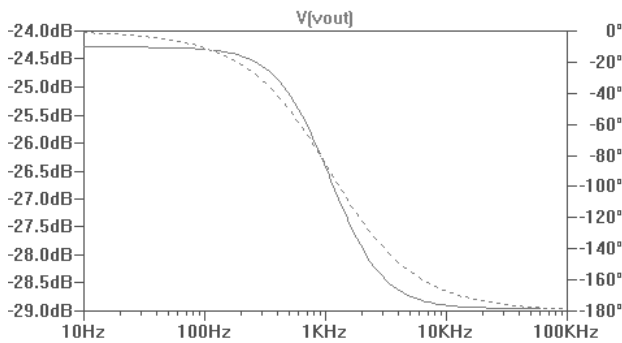


Fig.14.CCII- based Voltage mode all pass filter frequency response

$$I_x = 0 \quad (8)$$

Therefore networks have very high input impedance [10]. The filters are simulated using LTspice with 32nm CMOS parameters using CCII- implemented at 0.9V.

CONCLUSION

Positive and negative second generation current conveyor, CCII± was implemented in 32 nm CMOS technology, at 0.9V supply voltage. The circuits show current linearity of ±320µA and ±1mA, respectively. The dynamic range for both circuits varies from -600mV to 600mV. Voltage differentiators are presented using CCII+ and CCII-. Also CCII- is used as basic building block replacing op-amp in voltage mode all pass filter, yielding a phase shift from 0° to -180° from +180° to 0°.

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