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Design and Simulation of Multiphase Synchronous DC-DC Converter

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Abstract- ***The switched-mode dc-dc converters are some of the most widely used power electronic circuits for its high conversion efficiency, flexible and highly reliable output voltage. These converters are designed to regulate the output voltage against the changes in the input voltage and load current. In this paper, a simulink model of a three-phase DC-DC converter for power supply application is presented. Further, three-phase DC-DC buck converter operation is studied and analyzed. Effects of converter component like Land C are studied and their influence on transient response are also analyzed.***

Keywords— **Buck dc-dc converter, synchronous, PID controller, Pulse Width Modulation (PWM), Duty Cycle, Reliable, High efficiency, Matlab, Simulink.**

I. INTRODUCTION

In recent past we are witnessing enormous growth in electronic industry. This has led to new challenges in the design of power supplies for microprocessors [1]. It is predicted that future microprocessor may require current more than 100A at voltage of less than 1V. Switched mode power supplies are very important in industry today, and provide reliable and high efficiency solutions for a wide range of applications. Switched mode converters can be used in power supplies and battery charging circuitry for computers, electric tools, televisions, media tablets, smart phones, automobiles, and countless other electronic devices. One of the most popular converters for the consumer electronics industry is the DC-DC step−down converter, also known as the buck converter.

Switched mode DC-DC buck converters are some of the simplest and most widely used power electronic circuits to convert voltage from one level to lower level by switching action with high conversion efficiency. These converters are designed to regulate output voltage against the variations in input voltage and output current. This requires control methods to meet the demand.

In its simplest form conventional single stage buck converter consists of two switches, filter components viz, inductance and capacitance, load and source. The fig.1 shows the conventional single-phase buck converter. Here Sw1 can be implemented using any power electronics switching device viz, SCR, MOSFET, IGBT etc., depending on switching frequency and power handling capability. As the input is dc it is always preferred to use fully controlled devices viz, MOSFET or IGBT. Sw2 is a diode.

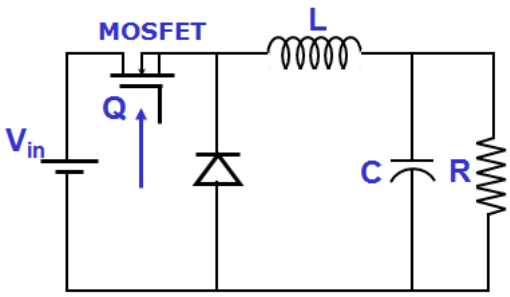

Fig. 1 : Conventional Buck Converter

In conventional buck converter, we use a series switch and a diode in shunt. This converter is used for conversion of much higher voltages to lower voltages. Here the output voltage is lowered to desired value by switching the main switch at high frequency alternating between (On and O FF) two states. Output voltage is the function of duty cycle which is the ratio of on time to total time of the switching cycle. Depending upon the required reduction in the output voltage, the duty cycle is calculated and accordingly the Mosfet and the Diodes are switched.

If the output voltage is very low like less than 1 volt, then it is better to go for second MOSFET device instead of diode. This configuration shown in fig. 2 is called as synchronous buck converter. This is done so as to reduce the power dissipation

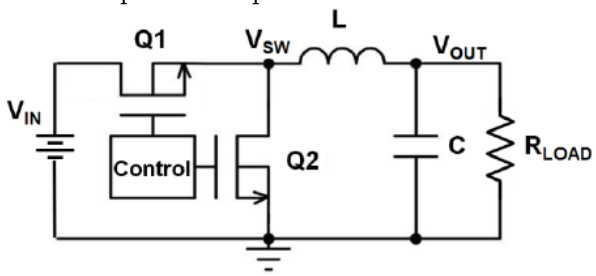

Fig. 2: Synchronous Buck Converter

To achieve better dynamic performance, multiphase interleaved converters are used, with small inductors and high switching frequency. However, the higher the switching frequency is, more is the power consumed. As a result, the efficiency of multiphase interleaved converters should be addressed separately [2]. Single-phase DC-DC converters do not meet this requirement.

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Hence several single-phase DC-DC converters are connected in parallel [3-4]. In parallel operation of 'n' single phases, each phase is staggered with displaced angle of 2π/n radians [4-6]

In this paper design of filter components to obtain high efficiency and fast dynamic response for three-phase DC-DC buck converter is presented.

II. Design of Filter Components:

The output stage of the synchronous buck converter consists of an inductor and capacitor as filter elements. The output stage stores and delivers energy to the load, and smoothens the output voltage. Selection of inductor directly influences the amount of current ripple on the inductor current, as well as the current capability of the buck converter itself. Inductors vary from manufacturer to manufacturer in both material and value, and typically have a tolerance of ±20%. Inductors have an inherent DC resistance (known as the DCR) that impacts the performance of the output stage. Minimizing the DCR improves the overall performance of the converter.

The output capacitance directly affects the output voltage of the converter, the response time of the output feedback loop, and the amount of output voltage overshoot that occurs during changes in load current. A ripple voltage exists on the DC output as the current through the inductor and capacitor increases and decreases. Capacitors also have a parasitic series resistance, known as the equivalent series resistance (ESR). The ESR impacts the output voltage ripple and the overall efficiency of the converter.

I. Design considerations:

Generally, multiphase VRMs are designed to supply high current at very low output voltage so as to take care of high density processors. At the same time, lower voltage helps Microprocessor operation easy. For designing a practical converter, we need to take into account the various parasitic effects of the components involved.

Following is the design specification for multiphase VRM .

Input Voltage, Vd = 12V
Output Voltage, Vo = 0.8V
Load Current, Io = 90A
Switching Frequency, fs = 400 kHz
Duty Ratio, D = 0.066

Peak-Peak ripple current is limited to 30% of load current, so ΔI = 27A

A. Calculation for Inductor.

For steady state operation, the change in current is given by

$$\Delta iL = \frac{(V_{IN} - V_O)DT_S}{L} = \frac{(V_O)(1-D)T_S}{L} \qquad (1)$$

By rearranging equation (1), we can find the value of the inductor as,

$$L = \frac{(V_{IN} - V_O)DT_S}{\Delta I_L} \qquad (2)$$

B. Calculation of Output Capacitor

The voltage ripple across the output capacitor is the sum of ripple voltages due to the "Effective Series resistance "(ESR), the voltage sag due to the load current that must be supplied by the capacitor as the inductor is discharged, and the voltage ripple due to the capacitor's ESL or "Effect Series Inductance". It is given by:

$$\Delta Vo = \Delta I \cdot \left(ESR + \frac{\Delta T}{C} + \frac{ESL}{\Delta T}\right) \qquad (3)$$

As the ESL specification is usually not specified by the capacitor vendor so the ESL value is assumed to be zero. At very high switching frequencies (>1 MHz), the ESL specification becomes more important.

Simplifying equation (3) by assuming ESL = 0:

$$\Delta V = \Delta I \cdot (ESR + \frac{\Delta T}{C}) \qquad (4)$$

Rearranging, we get

$$C = \frac{(\Delta I \cdot \Delta T)}{(\Delta V - (\Delta I * ESR))} (5)$$

The acceptable output voltage ripple, ΔVo, is defined as 8mV and ESR is selected as 0.03 Ω. Solving equation (5) with ΔVo =8mV, ΔI = 0.3 A, ESR = 0.03 Ω, and

Power loss in the capacitor is given by: (Iripple)2*ESR.

II. Selection of MOSFET

N-channel MOSFETs have advantages of lower on state resistance for a given die size and often have lower gate charge. They are inexpensive. Main drawback is – they require a boot strapped drive circuit, since the gate drive must be greater than the input voltage to the converter to enhance the MOSFET fully.

On the other hand, P – channel MOSFETs have simpler gate drive requirements. They require that their gate be pulled a few volts below the input voltage for them to be turned ON. The drawback is that their cost is higher as compared with N-MOSFET for the same RDS(ON) and they generally have slower switching times.

For lower side switch N-MOSFET with very low $R_{DS(ON)}$ is preferred.

III. Simulation results:

The fig.3 shows the circuit diagram of thee-phase synchronous buck converter for simulation.

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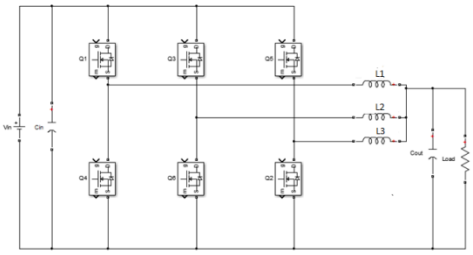

Fig. 3 : Simulation circuit of three-phase synchronous buck converter.

It consists of three main switches and three auxiliary switches. These switches are triggered at an interval decided by number of phases viz, 2π/n. where n is the number of phases. For n=3, phase displacement would be 1200.

The Fig.3.1 shows the gate pulses of three-phase synchronous buck converter.

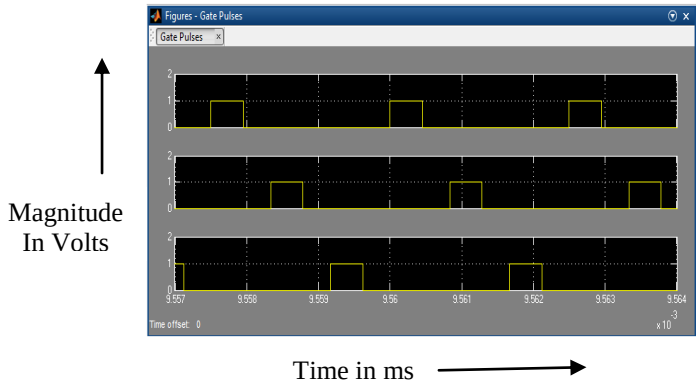

Fig. 3.1 : Gate pulses ror tnree-pnase synchronous buck converter.

We can observe that gate pulses are displaced by an angle 1200.

The Fig. 3.2 shows the phase currents and phase current ripples of three-phase synchronous buck converter.

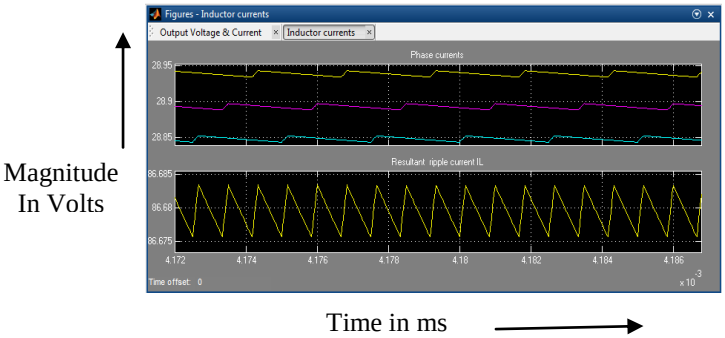

Fig. 3.2: Phase currents and phase current ripples of three-phase synchronous buck converter.

From the fig. 3.2 we observe that phase currents are displaced by 1200. This results in reduces load ripple current that results in reduced losses which improves the efficiency of the converter.

Fig. 3.3 shows the output voltage and output current of the three-phase synchronous buck converter.

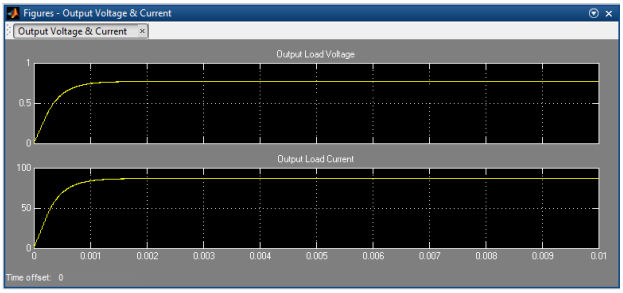

Fig. 3.3: Output voltage and output current of the three-phase synchronous buck converter.

From fig. 3.3 it is seen that the simulation results confirm with the design. Output voltage is 0.8V and output current is 87A. It is also observed that the ripple current reduces as the switching frequency increases and the settling time increases slightly with increase in switching time as shown in table 1. The same is shown in plots of fig. 3.4 and fig. 3.5 respectively.

TABLE 1.

RIPPLE CURRENT AND TRANSIENT RESPONSE ESTIMATION

Switching Frequency In kHz	Ripple Current In Amp	Settling time in msec
50	0.6	0.1
200	0.15	0.2
400	0.08	0.2

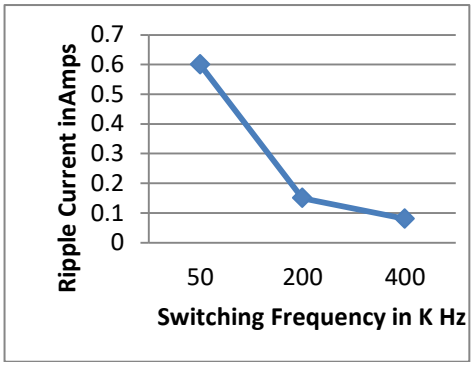

Fig..3.4: Graph of Ripple Current Vs Switching Frequency

Lower ripple current is always preferred as the losses in the converter reduce and converter efficiency increases.

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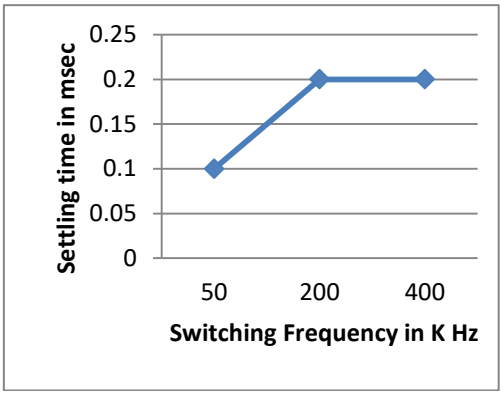

Fig. 3.5: Graph of Settling time Vs Switching Frequency

It is always preferred to have lower settling time. If settling time increases, transient losses also increase. Hence, to achieve desired efficiency and transient response, we need to optimally choose switching frequency, filter components and coupling coefficient.

TABLE 2.

LINE REGULATION

Sl. No	Input Voltage in(V)	Output Voltage in (V)	pu% error
1.	8	0.755	5.6
2.	9	0.76	5.0
3.	10	0.764	4.5
4.	11	0.767	4.1
5.	12	0.77	3.7
6.	13	0.772	3.5
7.	14	0.774	3.2
8.	15	0.775	3.1
9.	16	0.777	2.8

It is observed from TABLE 2, that for wide variation in input voltage, the output voltage remains fairly constant. This is shown in Graph 3.6.

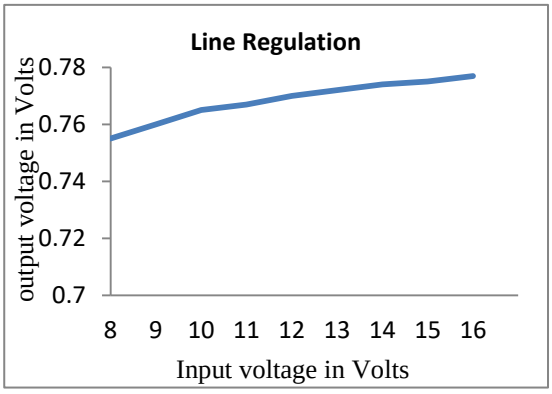

Fig. 3.6:. Graph of Line Regulation

TABLE 3

LOAD REGULATION

Sl. No	Output Current in (A)	Output Voltage in (V)	pu % error
1.	70	0.77	3.7
2.	75	0.77	3.7
3.	80	0.77	3.7
4.	85	0.77	3.7
5.	90	0.77	3.7
6.	95	0.77	3.7
7.	100	0.77	3.7
8.	105	0.77	3.7
9.	110	0.77	3.7

It is observed from TABLE 3, that for wide variation of load, the output voltage remains constant at 0.77 V. This is shown in Graph 3.7.

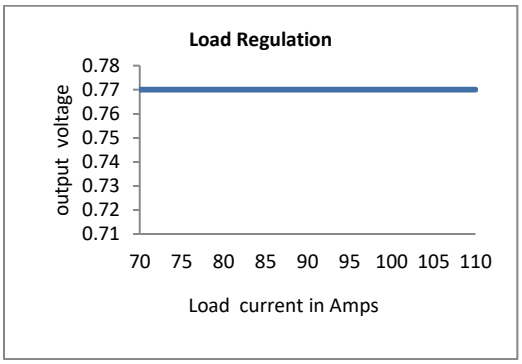

Fig.3.7. Graph of Load Regulation

IV. Conclusion

Design considerations for the 12V/0.8V, 90A three-phase synchronous DC-DC converter for VRM applications were presented. It is observed that for all switching frequencies, output voltage and output current remains constant at 0.77V and 88A respectively. It is also observed that, for wide variations in input voltage, output voltage fairly remains constant and also for load variations, output voltage remains constant at 0.77V. The design satisfies load and line regulations. The VRM power-stage design which can meet the specified efficiency and transient requirements were discussed.

V. Acknowledgment

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