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Realization of Universal Biquad Using Ultra Low Power DT-MOS Based CCII

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Abstract:- **An ultra-low-voltage, ultra-low-power active filter design using Dynamic Threshold MOSFET (DTMOS) based 2nd Generation Current Conveyer (CC-II) has been designed. The main feature of the proposed CC-II is that it is based on dynamic threshold MOS transistor (DTMOS). By connecting the body of a PMOS to the gate, the dynamic threshold MOSFET (DTMOS) in standard CMOS technology can be realised. The power consumption of proposed CC-II has been reduced to 0.42uW while all transistors are working in the sub threshold region. Universal filter is designed using the proposed CC-II circuit. The number of passive components used in these circuits is small, and voltage control characteristics are attractive. It is shown that these structures offer improvements in design simplicity and compared to op amp based structures as well as reduced component count. This work has been carried out using PSPICE Simulation software and the results obtained are in accordance with theoretical results.**

Keywords—**Analog signal processing, dynamic threshold MOS, Low-power circuit, Second-generation current conveyer Universal biquadratic filter, Voltage-mode**

I. INTRODUCTION

Now a days, the designing of current conveyer based active filters are of growing interest. This is ascribed to their greater linearity, high signal bandwidths, larger dynamic range than OPAMP based. Telecommunications, consumer electronics, radar, military ordnance and instrumentation systems make wide use of active filters. High-pass, Band-pass, Low-pass, notch and all-pass filters can be realized with the proposed voltage-mode circuit which has three inputs and two outputs.

By reducing the supply voltage, low power consumption requirement in digital designs can be achieved.This approach has caused significant performance losses in analog circuits where the decrease in threshold voltages does not follow the same trend of power supply reduction due to the leakage problems. Therefore, today's analog circuits, sharing same chip with their digital counterparts, suffer from the low-voltage levels of digital circuitry and relatively high threshold voltages which are not reduced below certain limits in standard CMOS process technology for keeping the leakage currents in acceptable ranges. This fact brings about the necessity of designing novel analog circuits that are suitable for low-voltage and low-power operation.

An important current mode building block is the current conveyer. There are three different generations of the current conveyer out of which second generation (CCII) is most widely used due to

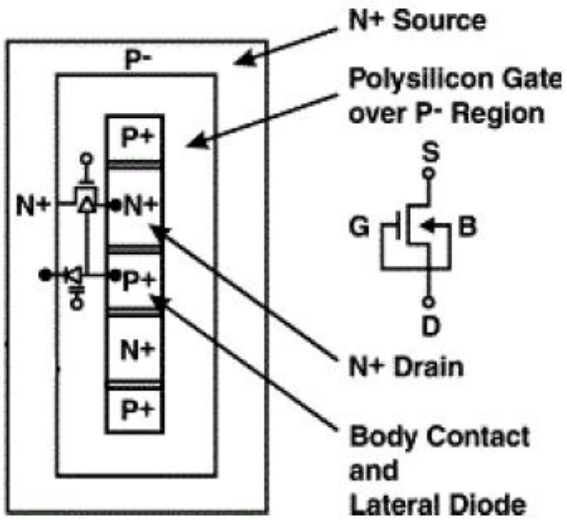

Fig.1: Dynamic Threshold MOS

Its versatile configurations. In this study, a dynamic threshold voltage MOS transistor (DTMOS)-based CCII circuit is proposed. More detailed explanations, additional simulation results and further mathematical derivations for the current conveyer and filter applications are given in this extended version.

II. DTMOS

In DTMOS technique the body and the gate of a DTMOS transistor are tied (or) biased at the same potential as shown in Fig. 1. When a high voltage is applied to the gate of a DTMOS transistor, the front channel of the device is turned ON [1].The body potential becomes high because the body is connected to the gate. The driving capability of the front channel increases because the threshold voltage becomes low due to the body effect.

When a low voltage is applied to the gate, the front channel turns off, so the body voltage becomes low, then due to the body effect, the threshold voltage of the front channel is recovered, thus the leakage current is small [2]. The threshold voltage reduces, as the gate and body voltage increase. With this DTMOS logic the transistor gets into "ON" mode at low VTH which results in the operation of circuit at low power and low voltages. The idea is to connect the gate and body of the device to dynamically change the threshold voltage of the transistor by utilizing the relation in [1].

$$V_{TH} = V_{TO} + \gamma(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}). \qquad (1)$$

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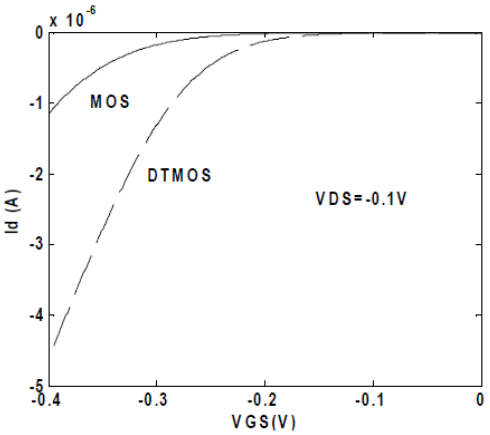

Fig.2: DTMOS and standard MOS drain currents[3]

DTMOS transistor, under the same VGS voltage behaves as a high-transconductance MOSFET. As it is seen in Fig. 2, it conducts more current than a regular MOSFET. In the figure, VDS kept at -0.1 V constant voltage while VGS is swept from -0.4 V to0V. The reason behind this mechanism is the threshold voltage reduction due to the positive source body voltage.

The possibility of very high forward biased junction currents of source body and drain body parasitic diodes is the main problem of such a connection. Because of this reason, DTMOS with its plain structure is useless for supply voltages exceeding 0.7V. Although it is possible to use it with an addition of an extra limiter transistor, this would almost double the chip area for digital circuits and additionally, it increases parasitic effects. Furthermore, the operation of all chip components strongly depends on those limiter transistors which decrease robust operation performance because any high on diode current totally disrupts transistor operation. For those reasons, supply voltages are chosen low enough to limit any forward biased diode currents in this study.[1]

III. DTMOS BASED CCII

An ultra low-voltage, ultra low-power, subthreshold CCII circuit has been designed using DTMOS transistors. The proposed circuit is depicted in Fig.3. The circuit structure is densely packed consisting of only eight transistors, all operating in the subthreshold region. The usage of only eight transistors increases the power consumption efficiency of the design and minimizes the parasitics as well. In the proposed CCII circuit in Fig.3, supply voltages are chosen as ± 0.2V and TSMC 0.18 µm process parameters are used in the design. Since the maximum bias voltage over the transistors is 0.4V, total bias voltage over the source body and drain body junctions of DTMOS transistors is limited which prevents latch-up problems caused by excess diode currents.

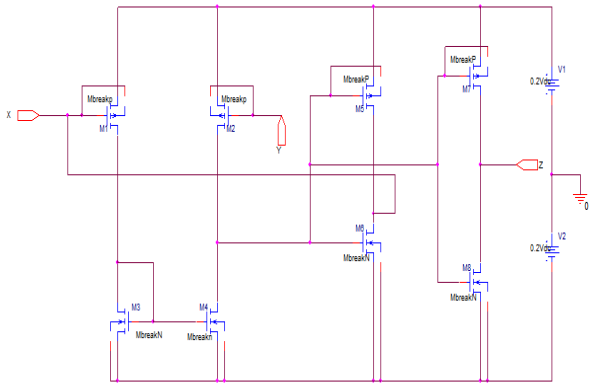

Fig.3: DTMOS-based ultra low-voltage, ultra low-power subthreshold CCII circuit.

The input stage of the CCII is formed by a pseudo differential low-voltage amplifier consisting of M1-M4.The output stage is the class AB stage from [1] with the modification of DTMOS transistor usage for ultra low-voltage operation. M1-M2 and M5, M7 are the p-MOS DTMOS transistors. There is feedback in the topology including M6 transistor which helps to decrease the resistance at the X input terminal which should be zero ideally. However, this is very difficult to achieve under subthreshold mode of operation where transistor transconductances are significantly low which severely affects the resistance seen at the X terminal.

Transistor aspect ratios of the circuit in Fig.3 are tabulated in Table 1. From Table 1, it can be claimed that relatively large transistors are used in the design. The reason is that they are chosen for correct operation of the circuit under ultra low supply voltage for the desired frequency range. This is generally the expected case for any MOS circuits operating in the subthreshold region with such low supply voltages where transistor dimensions have been chosen large to enable the flow of targeted current under ultra low-voltage operation.

The circuit is simulated by the program PSPICE. Fig.4 shows the input range where the V_X voltage follows V_Y voltage. The figure is obtained for a DC voltage source applied to the Y terminal while the X terminal is loaded with a 100k X load resistance.

From the Fig.4, it can be seen that the input voltage range is ± 60 mV with small following error. Defining a relative error term as,

$$\varepsilon = \frac{V_x - V_y}{V_x} \qquad (2)$$

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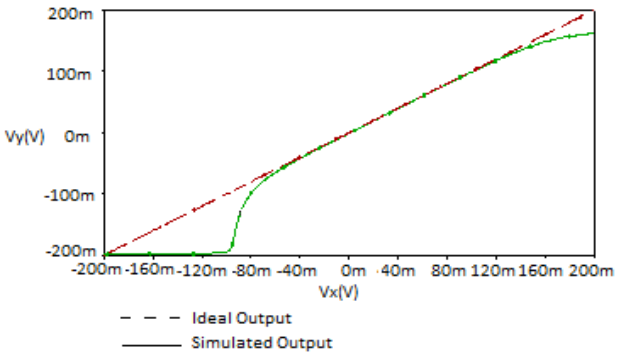

Fig.4 The change of V_X voltage versus V_Y voltage

Table 1: Transistor dimensions of the proposed CCII

Transistor	Width	Length
M1,M2,M5,M7	300 µm	02 µm
M3,M4	50 µm	02 µm
M6,M8	320 µm	0.4µm

IV. CCII based Universal filter

Considering the proposed voltage-mode circuit in fig.5, the nodal equations can be obtained as:

$$sC_1(V_{01} - V_1) + G(V_{01} - V_{02}) = 0 \quad (2)$$

$$G_1(V_{01} - V_{02}) + G_2(V_{02} - V_2) + sC_2(V_{02} - V_3) = 0 \quad (3)$$

$$V_{01} = \frac{s^2C_1C_2V_1 + s[C_1(G_2 - G_1)V_1 + C_2G_1V_3] + G_1G_2V_2}{s^2C_1C_2 + s(C_1G_2 + C_2G_1 - C_1G_1) + G_1G_2} \quad (4)$$

$$V_{02} = \frac{s^2C_1C_2V_3 + sC_2G_1V_3 + sC_1G_2V_2 - sC_1G_1V_1 + G_1G_2V_2}{s^2C_1C_2 + s(C_1G_2 + C_2G_1 - C_1G_1) + G_1G_2} \quad (5)$$

[2]From equations (3) and (4), we can see that:

i. If $V_2 = V_3 = 0$ (grounded), $G_1 = G_2$, V_1 = input voltage signal, a high-pass filter can be obtained at V_{01} and a inverted band-pass signal can be obtained at V_{02};
ii. If $V_1 = V_2 = 0$ (grounded), V_3 = input voltage signal, a band-pass filter can be obtained at V_{01};
iii. If $V_1 = V_3 = 0$ (grounded), V_2 = input voltage signal, a low-pass filter can be obtained at V_{01};
iv. If $V_3 = 0$ (grounded), $G_1 = G_2$, $V_1 = V_2$ =input voltage signal, a notch filter can be obtained at V_{01} and a low-pass signal can be obtained at V_{02};
v. If $V_3 = 0$ (grounded), $G_1 = 2G_2$, $C_2 = C_1$, $V_1 = V_2$ = input voltage signal, a all-pass filter can be obtained at V_{01};

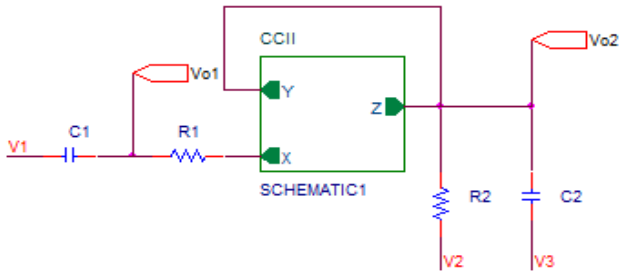

Fig.5 Proposed voltage – mode biquadratic Universal filter

vi. If $V_2 = 0$ (grounded), $C_2 = C_1$, $V_1 = V_3$ = input voltage signal, a high-pass filter can be obtained at V_{02}.

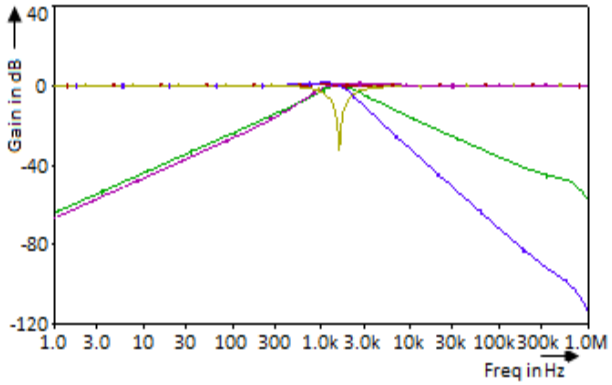

Fig.6 Universal filter output responses.

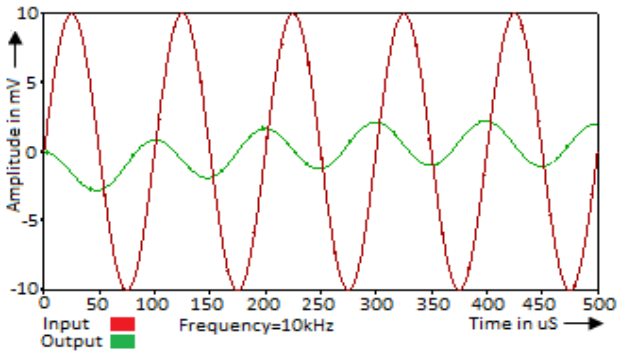

Fig.7 Time domain response for Inverted Band-pass filter

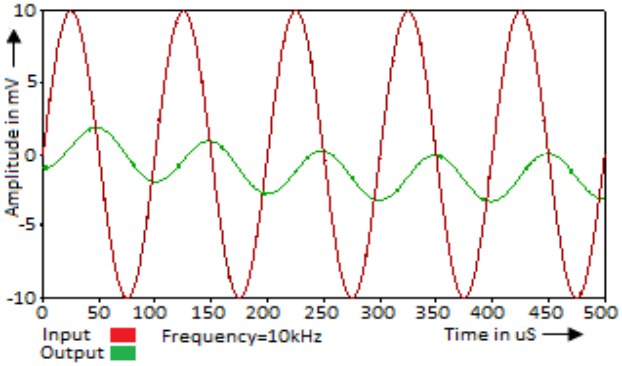

Fig.8 Time domain response for Band-pass Filter

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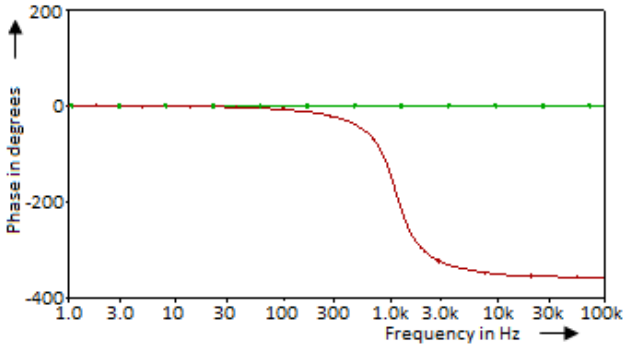

Fig.9 Phase and magnitude of All-pass filter.

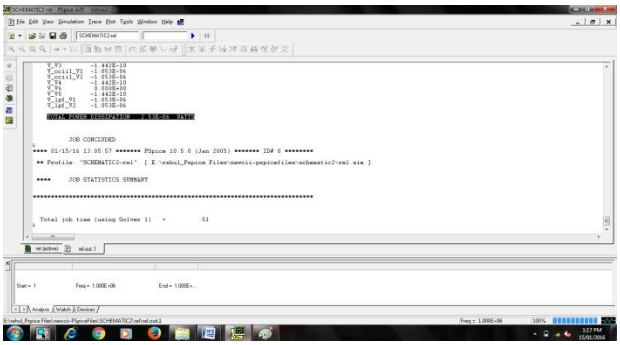

Fig. 10 Power Consumption of the proposed biquad.

The proposed biquadratic filter in fig.5 is a standard design for realization of all the filters viz. low-pass, high-pass, band-pass, inverted band-pass, band reject or notch filter and all-pass filter. Fig.6 shows the output of all the filters mentioned. The time domain response of inverted band-pass at 10 kHz is shown in Fig.7. The input signal is suppressed smoothly by inverted band-pass and band-pass filters in fig.7 and fig.8 respectively. In case of all-pass filter the phase and magnitude plot is as shown in fig.9.

CONCLUSIONS.

A voltage mode biquadratic filter has been presented. This circuit is implemented using only one DT-MOS CCII+ block and four passive elements. The total power dissipation of this filter is 2.53uW as per simulated results. Simulated results are well verified with the theoretical results.

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