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Grid Connected Single Phase Multilevel Inverter

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***Abstract*: - Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control, as they exhibit low total harmonic distortion (THD) in the output voltage and low electromagnetic interference (EMI). This paper presents a single-phase five-level inverter with pulse width modulation (PWM) technique for grid connection. Two triangular carrier signals identical to each other with an offset equivalent to the amplitude of the reference signal were used to generate PWM signals for the switches. The PWM technique proposed has some switches operated at fundamental line frequency and the others operate at inverter switching frequency. The advantage of the proposed inverter is that it requires less number of components and low THD compared with the conventional multilevel inverter. The inverter operational principles and the switching functions are analysed in this paper. Simulation results prove the powerful merits of the proposed multi-level inverter and the capabilities of the proposed PWM technique.**

Index Terms **— Multi-level Inverter, Multi-Carrier PWM, THD.**

I. INTRODUCTION

IN RECENT YEARS, industry has begun to demand higher power equipment, which now reaches the megawatt level. Multi Level Inverters (MLI) includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms [6]. Stepped output waveforms result in fewer harmonics in the output. This is one of the most desirous advantages of the Multi- Level Inverter now days. More the number of levels lesser are the step size. This makes the Inverter output voltage close to the sinusoidal voltage wave. MLI has two main advantages compared with the conventional H-bridge inverters [2], the higher voltage capability and the reduced harmonic content in the output waveform due to the multiple dc levels. The total harmonic distortion (THD) lowers down. MLI is now preferred in high power medium voltage applications due to the reduced voltage stresses on the devices [9]. MLI incorporates a topological structure that allows a desired output voltage to be synthesized among a set of isolated or interconnected distinct voltage sources. Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped); capacitor-clamped (flying capacitors) and cascaded multi-cell with separate dc sources [3], [4]. Along with the above advantages the multilevel inverter has some drawbacks. With the increased number of levels of the output voltage the number of switches used increases. This increases the cost and complexity of the circuit.

Many multilevel inverter topologies and their control techniques have emerged. The MLI technique implemented in [6] employs one switch and four power diodes to the H-bridge single phase inverter. The MLI technique implemented in [3] and [2] uses pulse width modulation (PWM) control algorithm with multicarrier signals. Another NPC/ H-bridge inverter employs multicarrier PWM technique that can reach to any required voltage levels with low number of carrier signals [7]. General rule for the phase-shift between the carrier signals of the adjacent modules in the modular photovoltaic grid-connected inverter controlled under phase-shifted carrier technique is proposed in [12].The paper [4] compares the operation of Neutral Point Clamped and H-bridge MLI with multicarrier technique with the phase shift of π/4 between the carrier signals.

This paper presents a single phase five level inverter with less number of components [2],[3].This reduces the gate drive circuits thus reducing the cost and complexity of the circuit. The five levels produced are: +2Vdc, +Vdc, 0, -Vdc, -2Vdc. This inverter uses two carrier signal and one modulating signal to generate PWM pulses. Some switches operate at switching frequency and some operate at fundamental frequency. The PWM Technique used is to reduce the switching losses and the harmonics.

Section II explains the principle of operation of the proposed Multi-Level Inverter. Section III explains the PWM strategy used for the inverter and section IV explains the switching algorithm that is used in PWM. The simulation results are described in section V to explain the operating principle of the inverter. Also a control circuit is designed to synchronize the inverter signal with the grid signal. However, the two power circuits are not connected to each other (the inverter operates isolated).

II. OPERATIONAL PRINCIPLE OF SINGLE PHASE MULTI-LEVEL INVERTER

The Five Level Inverter under consideration is shown in Figure 1. It consists of two cells; Cell-1 and Cell-2. Cell-1 consists of a dc source and two switches. One switch in series with the dc source and the other across the series connected dc source and the first switch.Cell-2 consists of only a dc source. The input dc source to the MLI can be a capacitor or a output of a solar PV cell or batteries.

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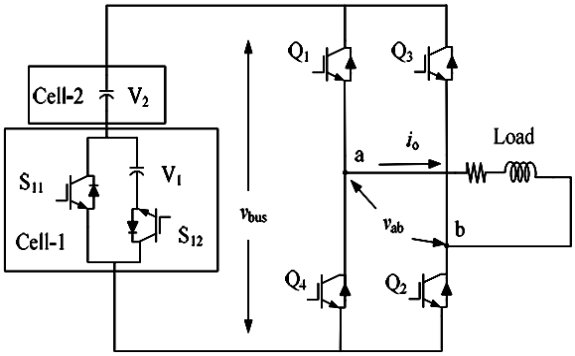

Figure 1. Proposed Single Phase Five Level Inverter

To obtain the voltage levels more than five at the output the number of cell-1 in series will increase accordingly. Switches S_{11} and $S_{12}$are switched ON to produce ±2Vdc and ±Vdc. The H-bridge inverter has four switches (Q_1, Q_2, Q_3 and Q_4). Switches Q_1 and Q_2 are operated to produce positive half cycle and switches Q_3 and Q_4 are operated to produce negative half cycle of the output voltage waveform. To obtain the zero voltage level either the upper two switches (Q_1, Q3) or the lower two switches (Q_2, Q4) are connected.

To generate the PWM pulses the five level inverter requires one modulating signal with amplitude A_m and two carrier signal each with equal amplitude A_c. The number of carrier signals depends on the number of DC link cells (n). Each carrier signal is shifted with carrier amplitude (A_c)from the former one. The amplitude of the modulating signal (A_m) can be varied from 0V to (n*A_c) according to the modulation index 0 to 1.

III. PWM Switching Technique

The operation of single phase five level inverter can be divided into ten switching states based on the direction of current as given in Table 1.

PWM is carried out with the help of a fully rectified modulating signal with amplitude A_m and two carrier signals each having amplitude A_c. One carrier signal is shifted from the former one by the carrier amplitude A_c as shown in Figure 2. Both the carrier signals are in phase. The amplitude modulation index for the five level inverter is

$$MI = \frac{Am}{2Ac} \quad (1)$$

Where,
A_m is the peak value of the modulating signal.
A_c is the peak to peak value of the carrier.

Table 1. Operational States of Switches

Switching States	Output Voltage (V_{ab})	Direction of Output Current (i_o)	ON State switches
1	Vdc	Positive	Q_1,Q_2 and S_{11}
2	Vdc	Negative	D_1, D_2 and S_{11}
3	2Vdc	Positive	Q1, Q2 and S12
4	2Vdc	Negative	D_1, D_2 and S_{12}
5	0	Positive	Q_1,D_3 or Q_2,D_4
6	0	Negative	D_1,Q_3 or D_2,Q_4
7	-2Vdc	Positive	D_3, D_4 and S_{12}
8	-2Vdc	Negative	Q_3, Q_4 and S_{12}
9	- Vdc	Positive	D_3, D_4 and S_{11}
10	- Vdc	Negative	Q_3, Q_4 and S_{11}

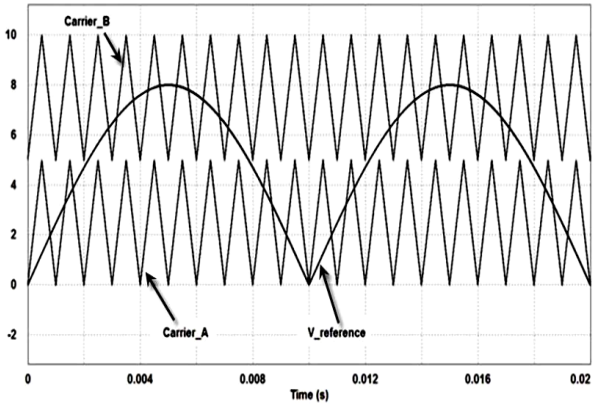

Figure 2. PWM Switching Strategy

The frequency ratio is given by

$$m_f = \frac{fc}{fm} \quad (2)$$

Where,
f_c is the frequency of the carrier signal.
f_m is the frequency of the modulating signal.

IV. PWM Switching Algorithm

In this paper PWM technique includes comparison of the amplitude of the rectified reference sinusoidal (modulation) signal with the two triangular (carrier) signals having same frequency and phase angle. When the amplitude of the modulating signal is less than that of the carrier signal, the modulation index is less than 0.5 (50%) and the inverter behaves similar to a conventional full bridge three level PWM inverter. This gives one level of output voltage. When the output is increased beyond the modulation index 0.5 modulating signal is compared with the upper carrier signal generating the second level of output voltage. Based on the modulation index; whether MI<0.5 or MI>0.5 the switching pattern of the proposed inverter is divided into following modes:

Mode A: $0 < \omega t \leq \theta_1$, $\theta_2 < \omega t \leq \pi$

Mode B: $\theta_1 < \omega t \leq \theta_2$

Mode C: $\pi < \omega t \leq \theta_3, \theta_4 < \omega t \leq 2\pi$ (3)

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Mode D: $\theta_3 < \omega t \leq \theta_4$

When the modulation index is more than 0.5 the phase angle displacements are

$$\left.\begin{aligned} \theta_1 &= \sin^{-1}\left(\frac{Am}{2Ac}\right) \\ \theta_2 &= \pi - \theta_1 \\ \theta_3 &= \pi + \theta_1 \\ \theta_2 &= 2\pi - \theta_1 \end{aligned}\right\} \quad (4)$$

When the modulation index is less than 0.5 the phase angle displacements are

$$\theta_1 = \theta_2 = \frac{\pi}{2}, \quad \theta_3 = \theta_4 = \frac{3\pi}{2} \quad (5)$$

The switching pattern of the proposed five level inverter is as shown in Figure 3. The comparators (CA and CB) compare the modulating signal with the respective carrier signal dividing one period of the reference signal into six intervals (P1, P2, P3, P4, P5 and P6) as shown in Figure 3(a). The generated output voltage is also shown.

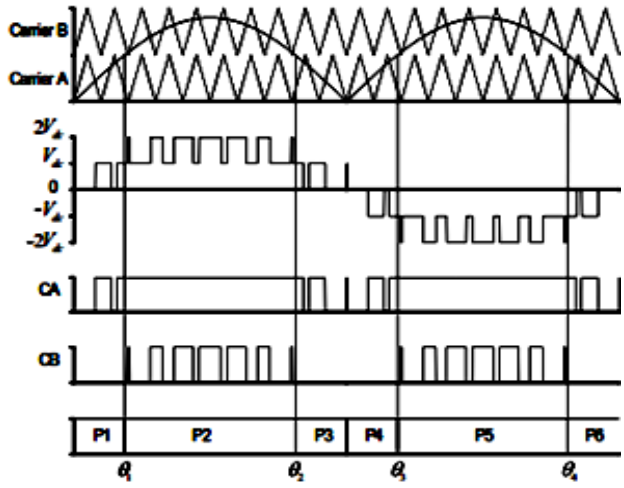

Figure 3(a): Comparator Control signal and Inverter Output Voltage Pattern in one cycle.

The control signals are generated by the control signals coming from the two comparators (CA and CB) as shown in Figure 3(b). Switches Q_1 and Q_4 operate at the fundamental frequency (50Hz). The switch S_{11} operates at high switching frequency. The switches Q_3 and Q_4 operates between low and high switching frequency, whereas the switch S_{12} operates at high frequency at some intervals and remain OFF elsewhere. The switching signals for the switches Q_1-Q_4 and S_{11}-S_{12} can be formulated

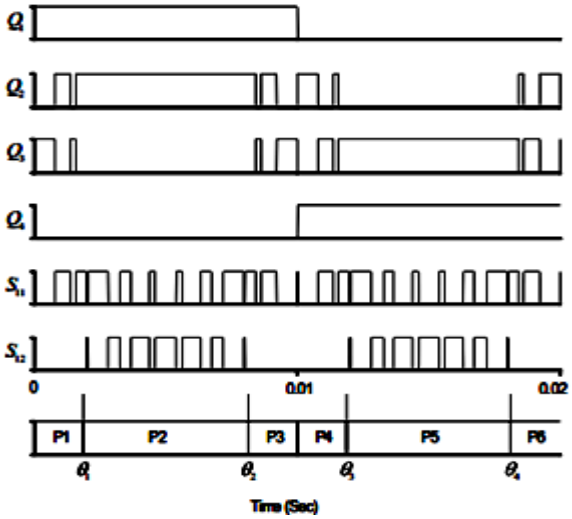

Figure 3(b): Gating Signals for the Inverter

based on the P_1, P_2, P_3, P_4, P_5, P_6 by the phase angle displacement using logical gates as given by equation (6).

$$\left.\begin{aligned} Q_1 &= (P1+P2+P3)\cdot CA \\ Q_2 &= ((P1+P2+P3)\cdot CA) + ((P4+P6)\cdot \overline{CA}) \\ Q_3 &= ((P1+P3)\cdot \overline{CA}) + ((P4+P5+P6)\cdot CA) \\ Q_4 &= P1+P2+P3 \\ S_{11} &= (((P1+P3)+(P4+P6))\cdot CA) + ((P2+P5)\cdot \overline{CB}) \\ S_{22} &= (P2+P5)\cdot CB \end{aligned}\right\} \quad (6)$$

The P1, P3 and P4, P6 are periods during positive half and negative half cycle respectively of the modulating or reference signal when the rectified modulating signal is less than or equal to the amplitude of the lower carrier signal. The P2 and P5 are the periods when the rectified modulating signal varies between the amplitude of the lower and upper carrier signal during positive and negative half cycles of the modulating or reference signal respectively.

There are two modes of working of the proposed inverter. They are:

1. The inverter operates when isolated from the grid.
2. The inverter operates when connected to the grid.

The proposed inverter has been designed for the isolated mode of operation. The output voltage of the inverter can be controlled by varying the frequency, magnitude and phase of the modulating signal.

V. Results And Discussion

The control circuit of the proposed inverter is designed for the isolation mode which means the inverter is not connected to grid. However the control signal from inverter output is compared with the reference (grid) voltage for comparison. The control circuit consists of a comparator that compares the control signal of the inverter output and the grid voltage and the error is processed accordingly to modify the amplitude modulation index, frequency and phase angle. The control

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circuit will perform the corrective action till the error signal is zero.

The proposed circuit is simulated in MATLAB SIMULINK as shown in Figure 4 to verify the performance of the proposed inverter circuit. A two cells (n=2) with five level output voltage waveform has been simulated. The switching frequency is selected as 15 kHz. Two identical power supplies of 26.5V each have been used for the dc bus. The dc bus voltage has been selected based on the desired inverter output voltage (<√2Vo; in this case the inverter output is 30Vrms). The modulation index will decide the shape of the inverter output voltage.

When the modulation index is less than 50% the inverter behaves like a conventional three level full bridge PWM inverter. In this case the lower cell is disconnected and the upper cell only is used to feed the load and the voltage and current waveform becomes flat at the peak. Thus the output voltage is not a pure sinusoidal waveform. When the MI lies between 0.5 and 1 the lower cell (cell-1) shares with the upper cell (cell-2) to supply the load producing a sinusoidal waveform at the output.

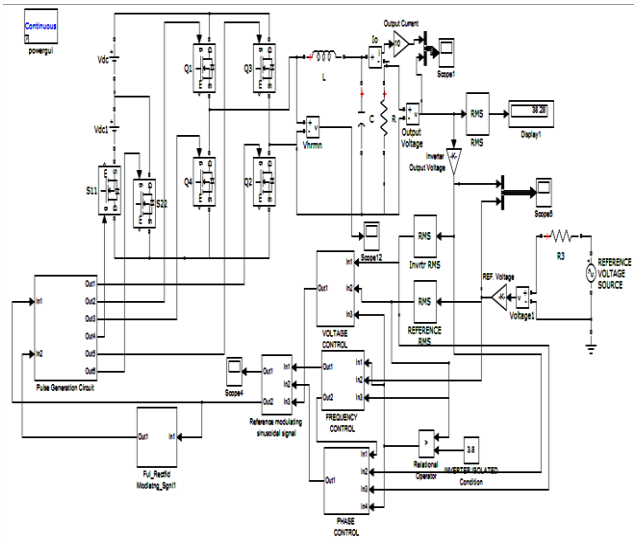

Figure 4.Circuit Schematic in SIMULINK

Figure 5 illustrates the inverter output, when isolated, at nominal MI (=0.8) and frequency.

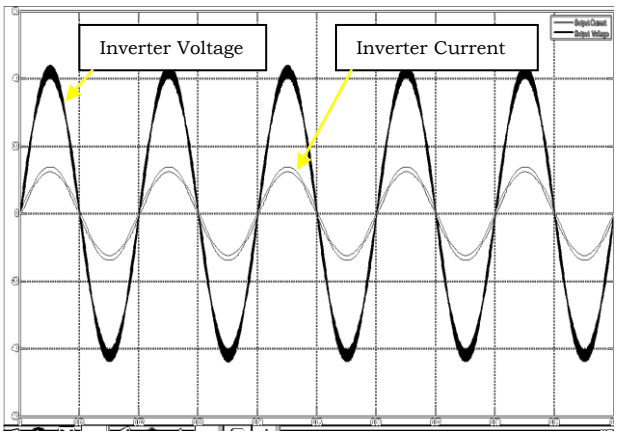

Figure 5. Inverter Output voltage and current at Vo= 30V, f= 50Hz , Φ=0°(MI=0.8)

In Figure 6 the inverter is operated in the isolated mode; independent of the grid supply. Figure 6(a) shows the inverter output voltage and current with Vo=33Vrms and frequency, f=51Hz, phase angle (with respect to grid control voltage) = 0°. The Figure 6(b) shows the inverter output voltage and current when the phase of the inverter with respect to reference (grid) control signal is 30° lagging. The Figure 6(c) shows the control signal of inverter voltage with respect to the grid control voltage when inverter output lags by 30°.

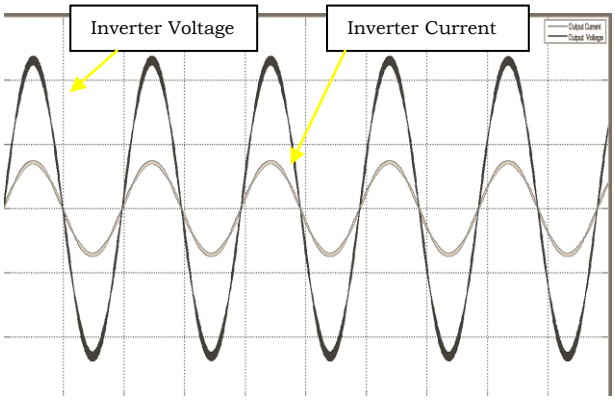

Figure 6(a): Inverter voltage and current with Vo=33V, f= 51Hz and Phase Angle=0°

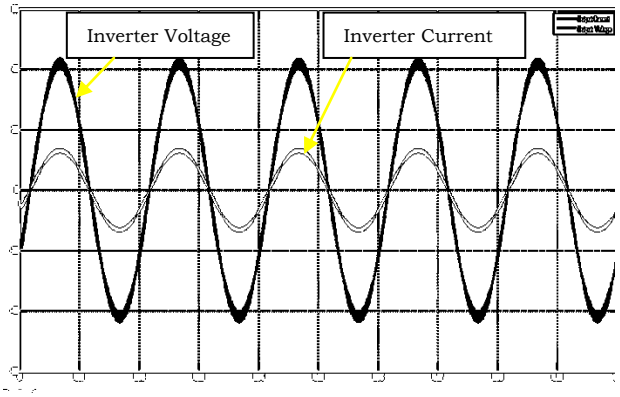

Figure 6(b): Inverter voltage and current with Vo=30V, f=50Hz and phase angle= 30°(lag)

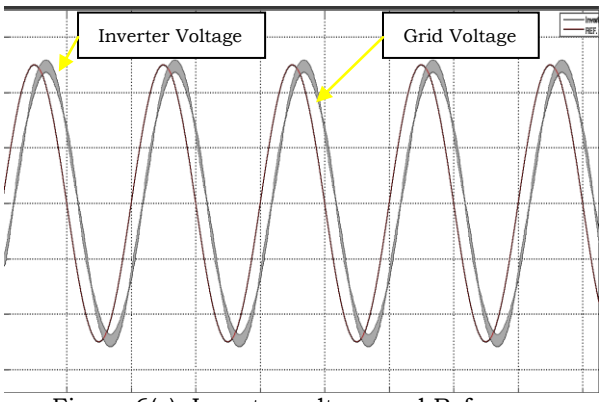

Figure 6(c): Inverter voltage and Reference (Grid)Voltage Waveforms.

When the control signal of grid is connected to the inverter already operating in isolated mode the inverter control signal follows the grid signal. Figure 7(a) depicts the inverter output voltage and current. However the grid is not connected to the inverter are isolated.

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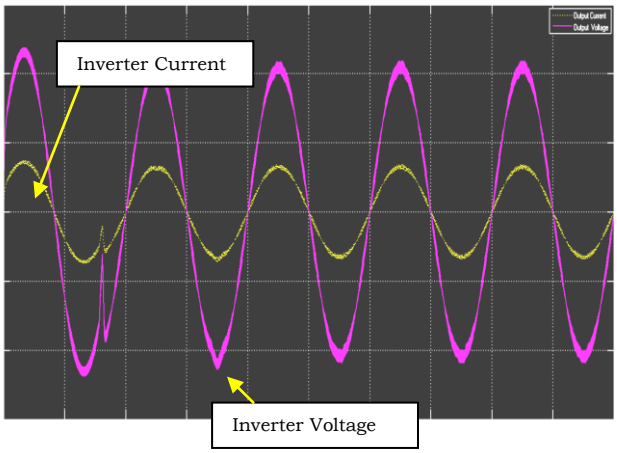

Figure 7(a): Inverter voltage and current waveforms when grid control signal is connected

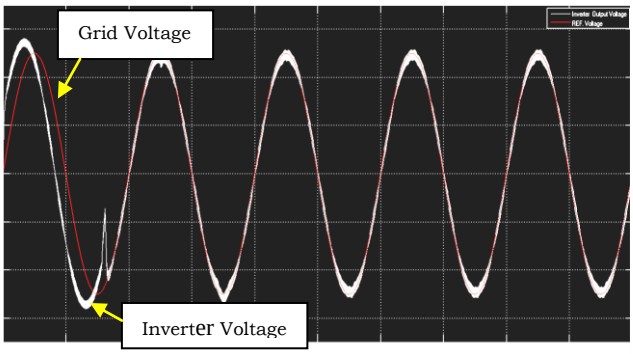

Figure 7(b): Inverter and Grid control voltage waveforms.

Figure 7(b) illustrates that the inverter control voltage follows the grid control signal and synchronizes with it after 2 to 3 cycles.

CONCLUSIONS

This paper has presented the five level inverter with less number of components as compared to the conventional H-bridge inverter. The THD is observed to be comparatively lesser. The inverter presented can be independently controlled. The proposed inverter has the capability to be connected to the grid. The future scope of this work is grid integration as the control signals are showing the results.

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