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Design of Current Controlled DVCC Based Floating Gate MOS and Its Application To Universal Filter

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Abstract: This paper proposes a new floating gate MOSFET (FGMOS) based Current Controlled Differential Voltage Current Conveyor (CCDVCC) structure using PSPICE model. Parameter used is 0.13µm TSMC CMOS technology for the NMOS and the PMOS transistors. Major advantage of FGMOS is Threshold voltage can be tuned using biasing circuits. The proposed circuit operates at the supply voltage of 0.5V. Less number of passive components are used in this circuit. As an application of CCDVCC a current controlled universal biquadratic filter (high pass, low pass, band pass, band reject and all pass) is presented. Simulation results are performed using ORCAD 10.5 by CADENCE.

Keywords — **floating gate MOSFET, current conveyor, and universal Biquad filter.**

I.INTRODUCTION

The trend towards low-power supply voltages is driven by lower power requirements. The speed and power consumption of CMOS circuits are reduced with the power supply voltage [10]. In order to maintain the speed we have to reduce the threshold of the MOS transistors. In this paper, a new FGMOS based CCDVCC is proposed to obtain flexibility in analog IC design. By using FGMOS transistors both the input stage of the circuit providing the arithmetic calculations gets simpler also the linearity range increases due to the properties of FGMOS differential amplifier. The proposed FGMOS based CCDVCC is used in a biquad in order to show the versatility of the this block. Both the FGMOS,CCDVCC circuit and KHN biquad are simulated with SPICE simulation program by using 0.13um technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

Low power and low voltage circuits are extensively demanded by the market of portable applications [10,11]. An alternative for these designs is using the floating gate transistors properties, whose main advantages lies on its simplicity and its possibility for connecting N control gates or secondary inputs in order to control its threshold voltage. These inputs are capacitively connected to the floating gate [12]. The idea is to control its threshold voltage to reduce the supply voltage and consequently the average power consumption without reducing the dynamic range.

The FGMOS technique has gained prime importance due to its ability to reduce or remove the threshold voltage requirement of the circuit. Threshold voltage reduction helps in reducing the supply voltage requirement and power dissipation in many analog applications.

The other advantage of FGMOS is its compatibility with standard double-poly CMOS process technology. The FGMOS transistors have found many applications in electronic programming [3], digital to-analog (D/A) and analog-to-digital converters [4], neural networks [5], voltage-controlled resistors [6]-[9], operational transconductance amplifier [10], multipliers [11], squarers [11]-[12], etc.

Rest of the paper is organized as follows. In Section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS based CCDVCC and simulation results of the proposed circuit are presented in Section III .The simulation results are shown in Section IV, respectively. A biquad filter, as an application example, is shown in section V followed by conclusion in section VI.

II. FGMOS

The first report of a floating-gate MOSFET was made in1967. There are various application of the FGMOS initially it was use to store digital data in EEPROM, EPROM and flash memories. The current interest in FGMOS circuits started from developing large-scale computations in neuromorphic systems, which are inherently analog.

The ccdvcc is employed by using floating gate mos.

The symbol and the equivalent circuit of an n-type FGMOS transistor with three inputs are shown in fig 1.Three input gate terminal of fgmos are FG1,FG2 and FG3. In this proposed circuit,the model is based on connecting capacitors in parallel with the resistors. Capacitance input CFG1, CFG2, CFG3

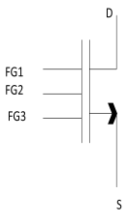

Figure 1: symbol

and input gate is coupled to floating gate of the FGMOS. CFGD, CFGS and CFGB are the parasitic capacitances between the drain, source, bulk and

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gate, respectively. Input gate voltages and drain, source and bulk voltages affect an effective floating gate voltage in proportion to value of the coupling capacitances. CT, sum of all the capacitances between the floating gate and the other terminals can be

$$V_{FG} = \frac{C_{FG1}V_{FG1} + C_{FG2}V_{FG2} + C_{FG3}V_{FG3}}{C_T}$$

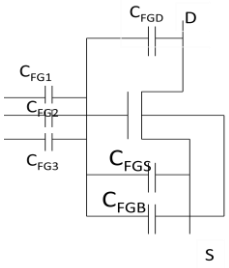

Figure 2: Equivalent circuit

The term C_T refers to the total sum of the capacitances seen by the FG, which is given by:

$$C_T = C_{GD} + C_{GS} + C_{GB} + \sum_{i=1}^{N} C_i$$

The drain current of the FGMOS in saturation region can be calculated as

$$I_D = \frac{k_n}{2}[V_{FG} - V_S - V_{TH}]^2$$

where V_S is the source voltage, V_{FG} is the effective floating gate voltage, V_{TH} is the threshold voltage and I_D is the drain current of the FGMOS transistor. In addition, K_n known as the transconductance parameter is $\mu n .Cox.(W/L)$ where W/L is the aspect ratio of the FGMOS transistor.

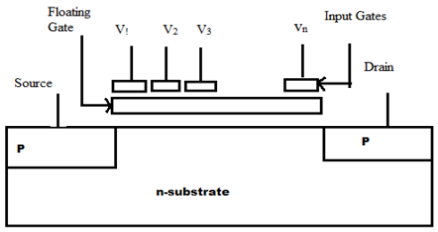

Figure 3 Structure of FGMOS

The basic structure of n-type, N-input FGMOS is shown
in Figure 2. Two layer of poly-silicon are formed. The first poly-silicon layer over the channel forms the floating gate and the second poly-silicon layer forms N-input gates that are located over the floating gate. V (for i = 1, 2,...,N) are the control input voltages and D, S and B are the drain, source and substrate, respectively.[13]

III. CCDVCC

Current controlled differential voltage current conveyor (CCDVCC) building block was introduced . CCDVCC is a widely used versatile analog building block whose applications exist in the literature.[5]
The CCDVCC is a four-port, widely used analog building block defined by the following matrix equation. [7]- [13]

$$\begin{bmatrix} V_X \\ I_{y1} \\ I_{y2} \\ I_z \end{bmatrix} = \begin{bmatrix} R_X & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_x \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix}$$

The circuit structure of the active block as introduced.
The FGMOS transistor based CCDVCC is shown in Fig 4.

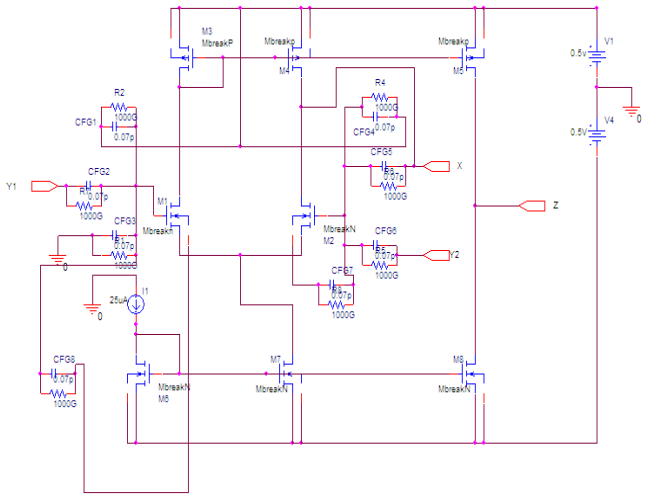

Figure 4 block diagram

A differential pair with transistors M4 and M5 FGMOS is designed . M1, M2 and M3 and the transistors M6, M7 and two separate current mirror with the transistor M8 is formed. Z
It must be equal to the current flow in the X terminal .Therefore, the transistor channel width of M1 and M2, M3 two times the width of the channel has been chosen as the transistor .

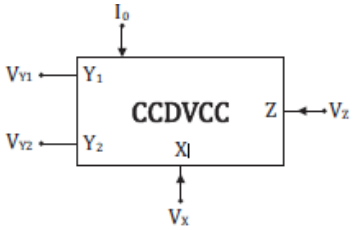

Figure 4.1

Type N, and a symbolic representation of the transistors FGMOS equivalent circuit is shown in Figure 1. The transistor FGMOS
The surroundings of the floating gate structure is covered with insulating oxide and the floating gate, the gate the source and base capacitive

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as a dependent. The effect on the output of the gate floating gate between them is proportional to the capacity. Here FG1, FG2 and FGN gate terminals D and S eluent is a source terminal.
Input capacity between floating gate to gate terminals.CFG1 is CFG2 and cfgn. The eluent, and source the base of the floating gate with the parasitic capacitance between them and
respectively CFGD is cfgsi and cfgb. These parasitic capacitances value is very small compared to input capabilities. Accordingly, the total capacity CT,

IV Simulation result and application.

The proposed ccdvcc was simulated by using SPICE model 0.13 µm TSMC CMOS technology parameter. This technology is used for the NMOS and the PMOS transistors. The aspect ratios of the MOS transistors, occurred in the ccdvcc implementation, are illustrated in Table I.
The supply voltage is ±0.5. The value of the capacitances CFG1, CFG2 and CFG3 can be taken as 0.07 pF.

Table 1: The aspect ratio of the MOS transistors.

Transistor	W(µm)	L(µm)
M_1,M_2	0.78	0.26
M_3,M_4,M_6,M_7,M_8	2.6	0.26
M_5	6.24	0.26

Table 1:Aspect ratio

For the proposed CCDVCC output displays the changing of the input voltage VY1 versus voltage VX.

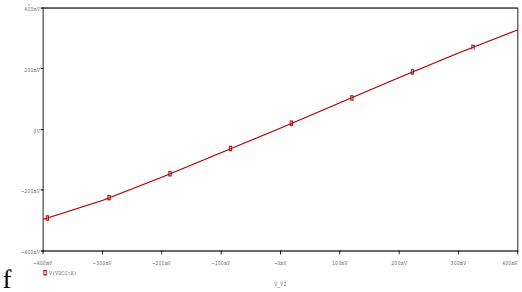

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Figure 5: Input voltage VY1 versus voltage Vx.

The graph has been obtained for the different values of the voltage VY2 as shown in Fig.6

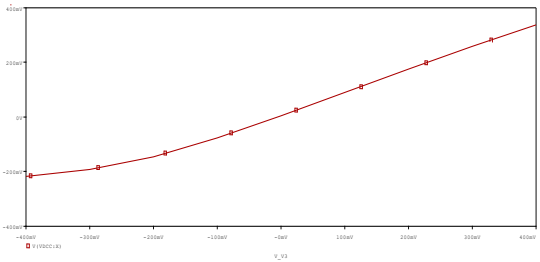

Figure 6: Different values of the voltage Vy2

The changing of the input current Ix versus current Iz for the CCDVCC is depicted in Fig. 7. Also, the transfer of current is linear from X to Z node

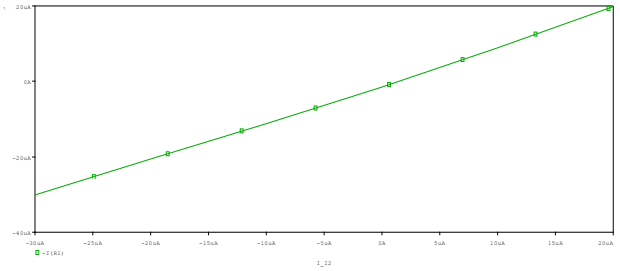

Figure 7 : Dc current

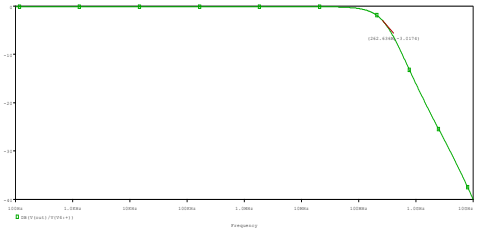

Figure 8: The frequency response of the voltage transfer gain for the proposed circuit.

The frequency response of the CCDVCC is shown in figure 8. Giving bandwidth of 262.635 MHz at 3db.

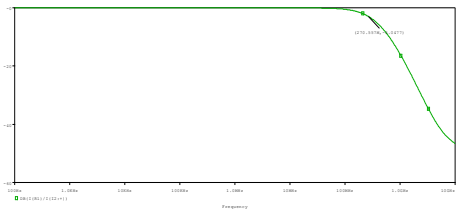

Figure 9: The frequency response of the current transfer gain for the proposed circuit.

.The cut-off frequency (-3 dB) is about 270.337 MHz as shown in figure 9.

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4 CCDVCC as biquad filter

Filter	V_1	V_2	V_3
Low pass	V_{in}	0	0
High pass	0	V_{in}	0
Band pass	0	0	V_{in}
Band reject	V_{in}	V_{in}	0
All pass	V_{in}	V_{in}	V_{in}

Table 2 conditions for filter

Consider the equivalent circuit of the CCDVCC filter circuit along with the expression of the transfer function.

$$V_o = \frac{V_2 S^2 C_1 C_2 R_{x1} R_{X2} + V_1 S C_2 R_{x2} + V_1}{s^2 C_1 C_2 R_{x1} R_{x2} + SC_2 R_{X2} + 1}$$

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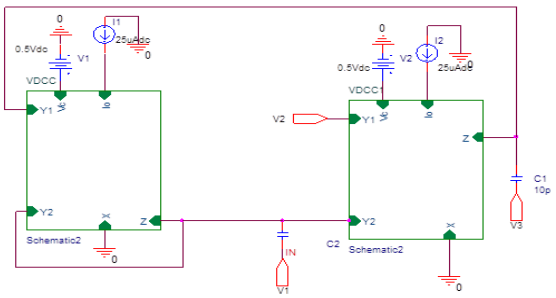

Figure 10 : proposed biquad universal filter .

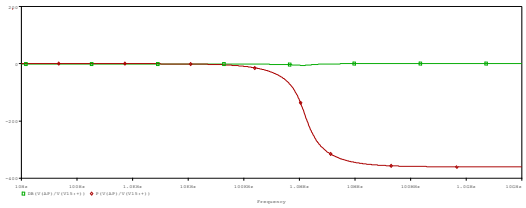

Figure 9 : All pass filter

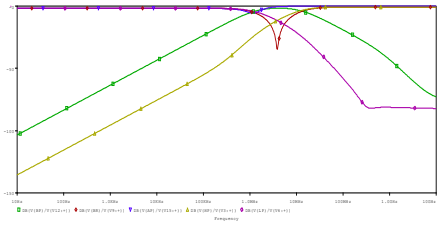

Figure 11: Universal filter

CONCLUSION

In this paper, a new approach called current controlled differential voltage current conveyor for realizing filters applications has been presented. Simulation results done by SPICE confirm the validity of the theory and demonstrate the use of the CCDVCC. FGMOS based the proposed circuit which has highly linear characterization shows that voltage transfer gain and current transfer gain. These values are admirable. Moreover, the frequency responses of the CCDVCC are acceptable levels. This CCDVCC is designed in 0.13 µm CMOS process and has $\square \pm 0.5\,V$ supply voltage.

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