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Design of biquad universal filters using BD-DDCC

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Abstract:- Enhancing the performance of analog circuits with sub-volt supplies becomes a great challenge for designers. This paper presents an ultra-low voltage CMOS topology for DDCC based on the Bulk Driven (BD) principle to design a universal bi-quadratic filter performing five simultaneous standard functions: All pass, band pass, low pass, band reject & high pass. The proposed circuit employs 2 BD-DDCC and minimum grounded passive elements. The performance of the proposed circuit is confirmed from PSPICE simulation results using the TSMC 0.18um CMOS technology to prove the functionality.

Keywords **- DDCC, filter, bulk driven (BD), CMOS.**

I. INTRODUCTION

In modern electronics, designs use low power analog signal processing and low voltage supply[1]-[3] to reduce the cost, size and weight of portable devices. Over the last few years, many techniques have been introduced in analog electronics literature Some of these techniques are quasi-floating-gate (QFG) bulk-driven (BD), floating-gate (FG), and other structures[3-7]. The BD principle was first presented in 1987[10]. Based on this principle, many interesting LV active building blocks were designed. In recent years, BD technique has attracted strong interest from researchers. In this paper, a new bulk driven based DDCC is proposed to obtain flexibility in analog IC design. The proposed Bulk driven based DDCC is used in a biquad in order to show the versatility of the this block. The BD-DDCC circuit and biquad are simulated with SPICE simulation Software by using 0.18 μm technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

II DDCC

The differential difference current conveyor (DDCC) was introduced in 1996 [8].It combines the good features of a differential difference amplifier (DDA), like low output impedance, high input impedance, low number of components, and capability of performing arithmetic operations, and the advantages of a current conveyor (CCII),such as bandwidth ,accuracy and high gain[8]. Therefore, the DDCC has been utilized in many interesting applications [11, 12, 13, 16-18].

The symbol of the DDCC is shown in fig.1

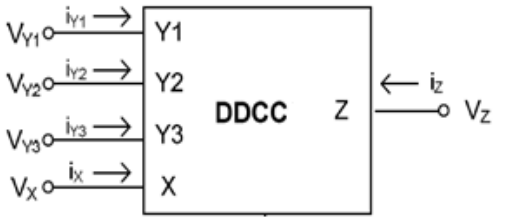

Fig:1 Equivalent circuit Diagram

The DDCC has 3 voltage terminals namely V_{y1},V_{y2} and V_{y3} which acts as a high input impedance and X terminal is low output current impedance terminal. Thus if realization connected between output terminal X and any input terminal Y, it will be acts as a low output impedance and high-input impedance.

The characteristics of DDCC is described in matrix relation is shown below:

$$\begin{bmatrix} i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_{Y1} \\ v_{Y2} \\ v_{Y3} \\ i_X \\ i_Z \end{bmatrix}$$

The circuit structure of the active block as introduced.The bulk drived based DDCC is shown in Fig 2

- Transistors M7, M8, M9, M10 and M_{13}act as a current mirror in which applying the constant current source *I*bias ie 5μA.
- It consists of 2 Bulk Driven differential input stages M3, M4 and M_1, M_2.
- Transistors M7 and M8 are common for both Bulk driven differential input stages.

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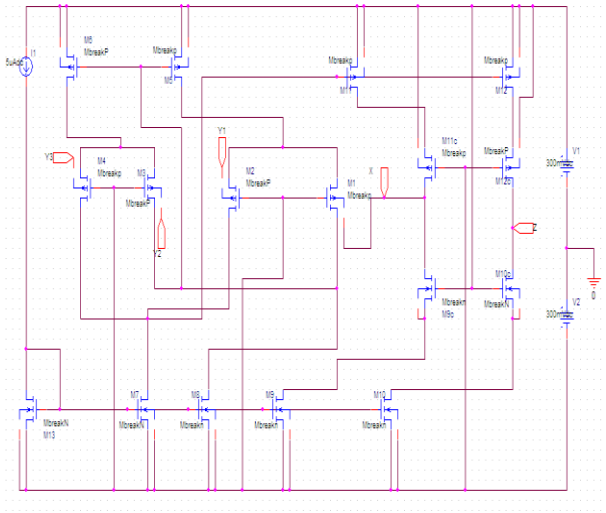

Fig:2 CMOS realization of DDCC

- M11, M11c and M9, M9c acts as a cascode transistors.
- Transistors M5 and M6 act as tail current Sources.

III Proposed Circuit

The proposed biquad circuit configuration in shown in fig. It consists of 2 DDCC's and 4 passive elements (2 capacitors and 2 resistors).

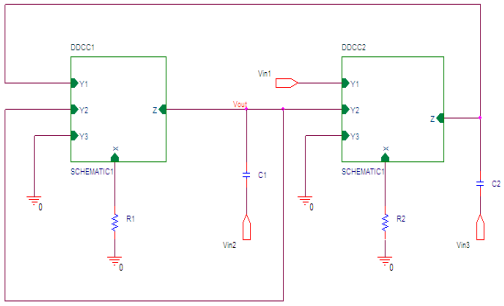

Fig:3 proposed biquad filter

The following transfer function:

$$V_{out}=\frac{S^4\,C_1.C_2\,.Vin2+S^2.\frac{C2}{R1}.Vin2+\frac{Vin1}{R1.R2}}{S^4(C_1.C_2)+S^2\left(\frac{C2}{R1}\right)+\frac{1}{R1.R2}}$$

Its is clearly seen from above equations:

- The all pass response can be obtained when $Vin_1=Vin_2=1$ and $Vin_3=-1$ and Vout is output.
- The band pass response can be obtained when $Vin_1=Vin_2=0$ (grounded) and $Vin_3=1$ and Vout is output.
- The low pass response can be obtained when $Vin_1=Vin_3=0$ (grounded)and $Vin_2=1$ and Vout is output.
- The band reject response can be obtained when $Vin_1=Vin_2=1$ and $Vin_3=0$ (grounded) and Vout is output.
- The high pass response can be obtained when $Vin_1=Vin_3=0$ (grounded) and $Vin_2=1$ and Vout is output.

The values of passive elements are $C_1=C_2=2nf$ and $R_1=R_2=10K\Omega$.The results obtained from the all pass, low pass, band pass, band reject and high pass realizations are shown in fig.

IV Simulation And Results

The proposed bd-ddcc was simulated by using SPICE model 0.18 µm TSMC CMOS technology parameter. This technology is used for the NMOS and the PMOS transistors. The aspect ratios of the MOS transistors, occurred in the bd-ddcc implementation, are illustrated in Table I.

The supply voltage $V_{DD}=0.3V$, $V_{SS}=-0.3V$ and $I_{BIAS}=5\mu A$.The value of the capacitances $C_1=2nF$ and $C_2=2nF$ and resistances $R_1=R_2=10K\Omega$.This values are designed to obtain AP,BP,LP,BR and HP filters. For the proposed BDDDCC output displays the port relationships of ports with respect to V_X.

The DC curves V_X versus V_{Y1} is shown in fig 4. In this response V_{Y2} and V_{Y3} are connected to ground and V_{Y1} is varies from -350mV to 350Mv. The output X also varies the input V_{Y1} but at certain voltage (250 mV) it can diverged. The DC curves Vx versus V_{Y2} is shown in fig 6. In this response input varies from -350 to 350mVsame as the V_{x1}. frequency responses of the voltage gains V_X/V_{Y1} and V_X/V_{Y2} ,is shown in fig 5 .The current gain and low frequency voltage are equal to 1 and their -3dB bandwidth is 42MHz.The DC curve I_X versus I_Z is shown in fig 7. Here I_Z follows the input I_X but after 5µAmp (biasing current). The frequency response of current gain IZ/IX is shown in fig.8.and its -3dbbandwidth is 596KHz.

Transistor	W(µm)	L(µm)
M1,M2,M3,M4	100	0.3
M5,M6	50	0.3
M7,M8,M13	4	0.3
M9,M10	8	0.3
M11,M12	100	0.3
M9C,M10C	50	2
M11C,M12C	100	2

TABLE1: Transistors aspect ratios and component values

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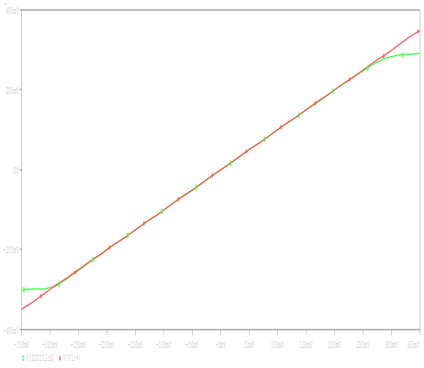

Fig:4 Input voltage V_{Y1} versus V_x

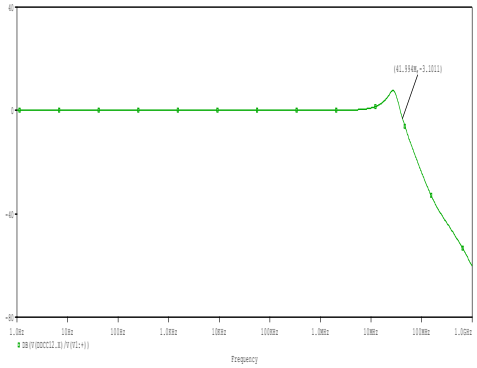

Fig5: Frequency responses of voltage gains VX/VY1, VX/VY2

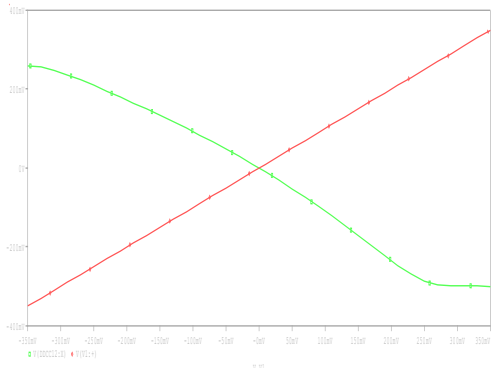

Fig.6 Input voltage V_{Y1} versus V_x

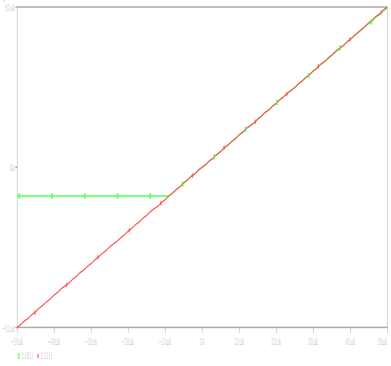

Fig.7 DC curve I_X versus I_Z

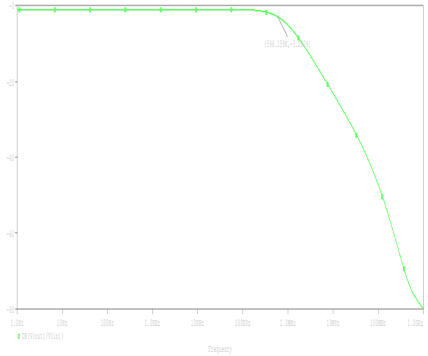

Fig.8. frequency response of current gain I_Z/I_X

The simulated results for the AP,LP,BP,BR and HP filters characteristics are shown below fig.9. The frequency at whish all these filters are worked properly is 10 KHz which is shown in fig 9. The frequency response of phase and gain of all pass filter is shown in fig10. The input and output response of band pass filter for 1KHz is shown in fig.11.

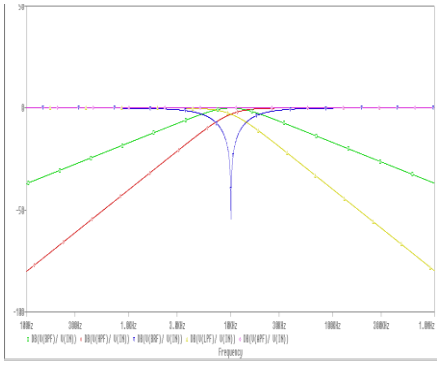

Fig :9 Frequency response of AP,LP,BP,BR and H Pin db

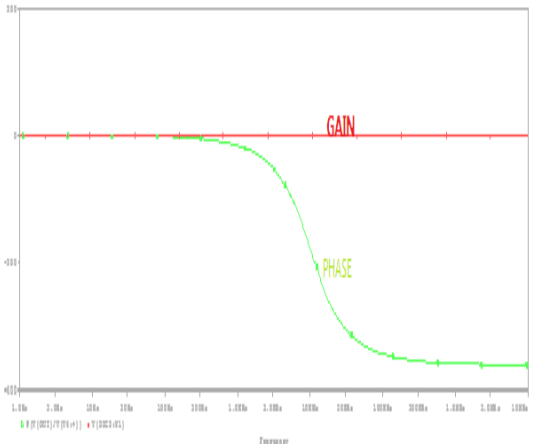

Fig10. Phase and Gain response of AP filter

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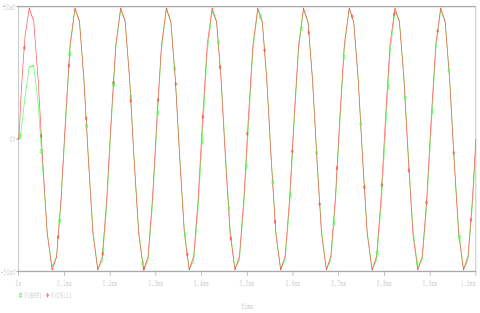

fig:11 The input and output response of BP filter

CONCLUSIONS

In this paper, a new approach called differential difference current conveyor for realizing filters applications has been presented.Simulation results done by PSPICE confirm the validity of the theory and demonstrate the use of the DDCC.

REFERENCES

[1] SERDIJN, W. A., BROEST, M., MULDER, J., VAN DER WOERD, A. C., VAN ROERMUND, A. H. M. A low-voltage ultra-low-power translinear integrator for audio filter applications.IEEE Journal of Solid-State Circuits, 1997, vol. 32, p. 577–581

[2] J.M. Carrillo, G. Torelli, R. Pérez-Aloe, J.M. Valverde, J.F. Duque-Carrillo, Single-pair bulk-driven CMOS input stage: a compact low-voltage analog cell for scaled technologies. Integration VLSI J.43, 251–257 (2010)

[3] FERRI, G., GUERRINI, N. High-valued passive element simulationusing low-voltage low-power current conveyors for fully integratedapplications. IEEE Transactions on Circuits and Systems-II,2001, vol. 48, p. 405–407.

[4] LAOUDIAS, C., PSYCHALINOS, C. Universal biquad filtersusing low-voltage current mirrors. Analog Integrated Circuits and Signal Processing, 2010, vol. 65, p. 77–88.

[5] A. Guzinski, M. Bialko, J.C. Matheau, Body-driven differential amplifier for application incontinuous-time active C-filter, in Proc. ECCD, Paris, France (1987), pp. 315–319

[6] Y. Haga, I. Kale, Bulk-driven flipped voltage follower, in Proc. IEEE ISCAS (2009), pp. 2717–2720S.-W. Pan, C.-C. Chuang, C.-H. Yang, Y.-S. Lai, A novel OTA with dual bulk-driven input stage, in Proc. ISCAS 2009 (2009), pp. 2721–2724

[7] P. Prommee, M. Somdunyakanok, CMOS-based current-controlled DDCC and its applications to capacitance multiplier and universal filter. AEÜ, Int. J. Electron. Commun. 65, 1–8 (2011)

[8] W. Chiu, S.I. Liu, H.W. Tsao, J.J. Chen, CMOS differential difference current conveyors and their applications. IEE Proc., Circuits Devices Syst. 143, 91–96 (1996)

[9] W.-Y. Chiu, J.-W. Horng, Voltage-mode highpass, bandpass, lowpass and notch biquadratic filters using single DDCC. Radioengineering 21, 297–303 (2012)

[10] A. Guzinski, M. Bialko, J.C. Matheau, Body-driven differential amplifier for application in continuous-time active C-filter, in Proc. ECCD, Paris, France (1987), pp. 315–319

[11] 3. H.P. Chen, Universal voltage-mode filter using only plus-type DDCCs. Analog Integr. Circuits Signal Process. 50, 137–139 (2007)

[12] H.P. Chen, K.H. Wu, Single DDCC-based voltage-mode multifunction filter. IEICE Trans. Fundam. Electron. Commun. Comput. Sci. 90-A, 2029–2031 (2007)

[13] H.P. Chen, Versatile universal voltage-mode filter employing DDCCs. AEÜ, Int. J. Electron. Commun. 63, 78–82 (2009)

[14] W.Y. Chiu, J.W. Horng, High-input and low-output impedance voltage-mode universal biquadratic filter using DDCCs. IEEE Trans. Circuits Syst. II, Express Briefs 54, 649–652 (2007)

[15] W.-Y. Chiu, J.-W. Horng, Voltage-mode highpass, bandpass, lowpass and notch biquadratic filters using single DDCC. Radioengineering 21, 297–303 (2012)

[16] J.-W. Horng, High input impedance voltage-mode universal biquadratic filter with three inputs using DDCCs. Circuits Syst. Signal Process. 27, 553–562 (2008)

[17] M.A. Ibrahim, H. Kuntman, O. Cicekoglu, Single DDCC biquads with high input impedance and minimum number of passive elements. Analog Integr. Circuits Signal Process. 43, 71–79 (2005)

[18] W.-T. Lee, Y.-Z. Liao, New voltage-mode high-pass, band-pass and low-pass filter using DDCC and OTAs. AEÜ, Int. J. Electron. Commun. 62, 701–704 (2008)

[19] Fabian Khateb, Montree Kumngern, Vlassis Spyridon · Costas Psychalinos, Differential Difference Current Conveyor Using Bulk-Driven Technique for Ultra-Low-Voltage Applications. (online) 18 June 2013 Springer Science+Business Media New York 2013

[20] Montree KUMNGERN 1, Fabian KHATEB 2, Kobchai DEJHAN 1,Pattarapong PHASUKKIT 1, Supan TUNGJITKUSOLMUN 1, Voltage-Mode Multifunction Biquadratic Filters UsingNew Ultra-Low-Power Differential Difference Current Conveyors