Closed-loop speed control of bridgeless PFC buck- boost Converter-Fed BLDC motor drive

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Abstract - **This paper presents performance analysis closed loop speed control of bridgeless (BL) power factor corrected (PFC) buck-boost converter fed brushless direct current (BLDC) motor. A wide range of torque and speed control of the electric motor is required in most applications. The use of brushless direct current motor (BLDC) in household applications is becoming very common due to high efficiency, fast response, low inertia and low maintenance. Conventional schemes use diode bridge rectifier at the front end but the proposed single stage PFC converter not only eliminates the conventional system of bridge rectifier but also increases power quality at ac mains. Hence PFC BL buck-boost converter is operated in discontinuous inductor current mode (DICM).The performance of the proposed drive is evaluated for a wide range of speed by carrying out simulation in PSIM environment.**

Index terms - Bridgeless (BL), buck-boost converter, Brushless direct current (BLDC), discontinuous inductor current mode (DCM), power factor converters (PFC)

I. INTRODUCTION

The use of BLDC motor in recent times is gaining a lot of interest due to its high efficiency, fast dynamic response, high flux density and low maintenance in household applications like fans, water pumps, mixers, exhaust fans etc. The use of BLDC motor is not only limited to household applications it is also used in Locomotives, Medical equipments, Industrial tools and Aerospace applications.

BLDC motors use hall sensor based rotor position detection for the electronic commutation which is an advantage over mechanical commutation, due to the absence of brushes and commutator which increases the span of the motor hence can be used even for high speed ranges.

Conventionally the BLDC motors are fed from single phase AC supply through diode bridge rectifier (DBR) followed by high DC link capacitor. It draws peak current which results in total harmonic distortion (THD) of supply current of the order of 81.54 % and a poor power factor (PF) around 0.728. Hence PFC converters are used after DBR to improve the power factor. Further many single stage AC-DC PFC converters are reported in the literature survey which gained more importance due to low component count and minimal number of switches are required to control DC link voltage.

One has to consider the mode of operation of PFC converter which directly affects the cost and device rating which is the main concern in low power applications. The converter mainly operates in two modes - Continuous conduction mode (CCM) & Discontinuous conduction mode (DCM). In CCM, the current through the inductor or the voltage across the DC link capacitor remains continuous, but it requires 3 sensors for PFC operation. Hence it is not cost-effective. On the other hand, DCM requires only one voltage sensor for dc link voltage control, hence DCM is preferred for low-power applications.

Conventional control of the BLDC motor drive utilizes pulse width-modulated voltage source inverter (PWM-VSI) for speed control with a constant dc link voltage. Hence, this method is not preferred as the switching losses increases with square of the switching frequency in VSI.

Many converters are proposed to improve the power factor (PF) at AC mains but has a drawback in one or other way. PFC buck, Boost & Buck-Boost converter operating in CCM[1-3]. The buck and boost converter limits the operating range of the dc link voltage and has a drawback of high switching losses. Further to this SEPIC converter was proposed. Though it is operated in DCM mode it also has high switching losses and high component count[4]. Later CUK converter based variable DC link voltage was proposed to operate in CCM (3 sensors) which is not cost effective in lower power applications[5].

Further to this BL PFC converters are proposed which completely eliminates the use of DBR in the front end[6-9]. Among all the converters, Buck-Boost converter is best suited for low power applications since it uses less components and currents flows through minimum number of components during half cycle of conduction. The following table gives the comparative study of various bridgeless configuration.

Configuration	Switch Sw	Diode D	Inductors L	Capacitance C	Total	Half period Conduction
BL-Buck	2	4	2	2	10	5
BL-Boost	2	2	1	1	6	4
BL-CUK T-1	2	3	3	3	11	8
BL-CUK T-2	2	2	3	4	11	11
BL-CUK T-3	2	4	4	3	13	7
BL-CUK	2	3	3	2	10	8
BL-SEPIC	2	3	1*	2	9	7
BL-SEPIC	2	3	2	2	9	7
PROPOSED	2	4	2	1	9	5

Table 1: Different PFC configuration with component counts

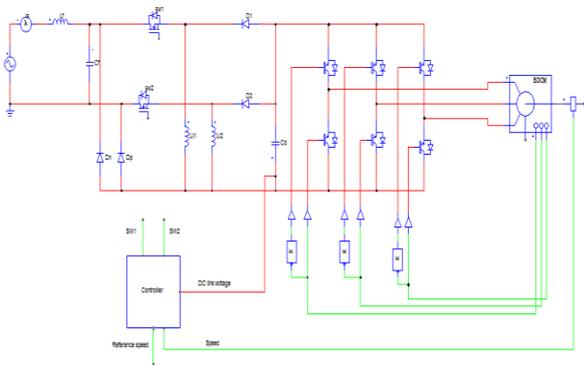## II. PROPOSED PFC BL BUCK-BOOST CONVERTER-FED BLDC MOTOR

Figure 1: Proposed PFC BL Buck-Boost converter-Fed BLDC motor

The figure shows proposed methodology comprising at the front end Buck-Boost converter followed by VSI fed BLDC motor. The converter parameters are designed such that it is made to operate in DCM, which results in improved PF at AC mains. The speed of the BLDC motor is directly proportional to DC link voltage. Hence by varying the voltage the speed can be controlled which reduces switching losses in VSI due to low frequency of operation of VSI. Further closed loop speed control is designed and the circuit is analyzed for various mechanical loads.

III. OPERATION OF BUCK-BOOST CONVERTER

The converter is operated in both positive and negative cycles. During positive cycle S_{w1} & inductor L_{i1}, and diodes D_1 and D_p are operated to transfer energy to dc link capacitor Cd. On the other hand, in negative half cycle of the supply voltage, switch S_{w2}, inductor L_{i2}, and diodes D_2 and D_n conduct to transfer energy.
There are three modes to complete a switching period in both the cycles.

Mode 1: In this mode, switch S_{w1} is triggered to charge inductor current to IL1 and diode D_p completes the cycle. In the meantime the capacitor Cd is discharged by VSI-Fed BLDC motor.
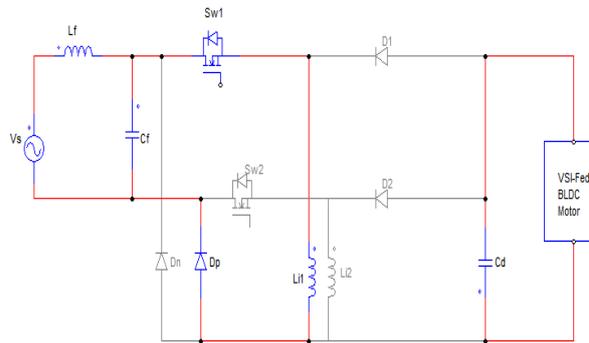

Fig 2(a)

Mode 2: In this mode, the S_{w1} is turned off and inductor energy is transferred to capacitor C_d. Hence the current in the Inductor reduces and reaches zero.
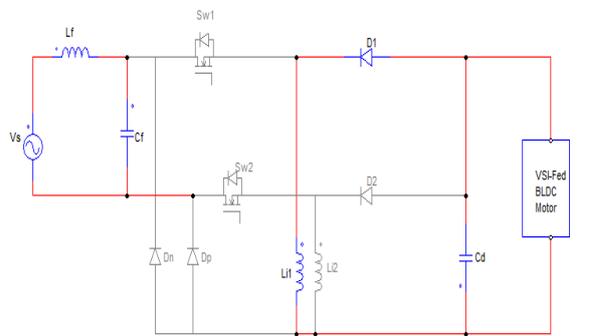

Fig 2(b)

Mode 3: In this mode, inductor L_{i1} enters discontinuous current mode. None of the switches or diodes conduct during this mode. Hence DC link capacitor transfers its energy to load and the DC link voltage V_{dc} starts decreasing. The operation is repeated when Sw1 is again turned on after a switching cycle.
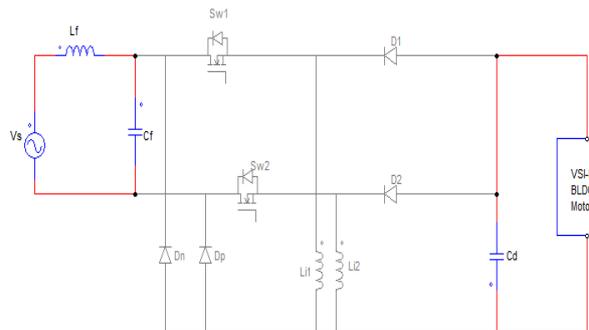

Fig 2(c)

Similarly, for the negative half cycle switch S_{w2}, inductor L_{i2}, and diodes D_n and D_2 operate for voltage control and PFC operation.
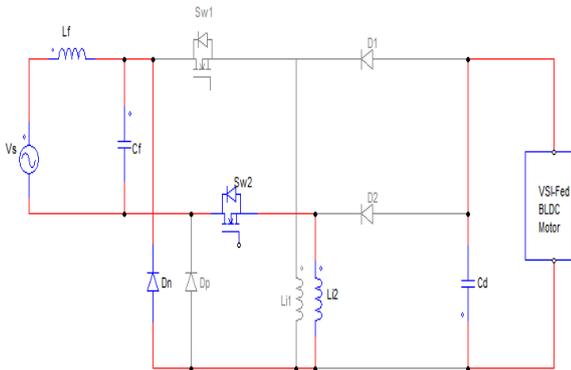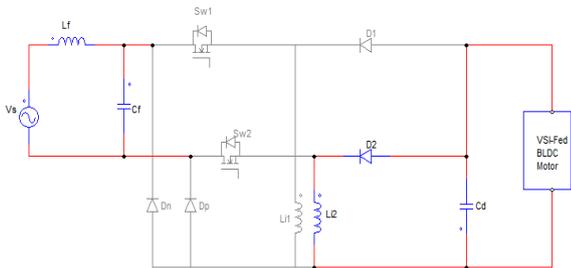
Mode 1:

Fig 2(d)

Mode 2:

Fig 2(e)

Mode 3:

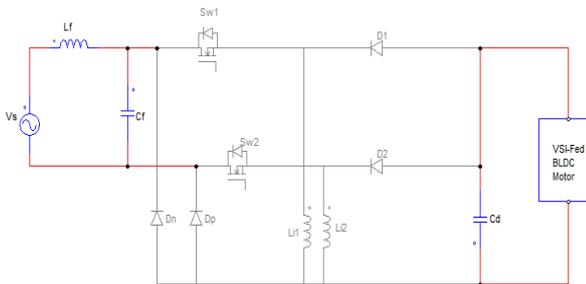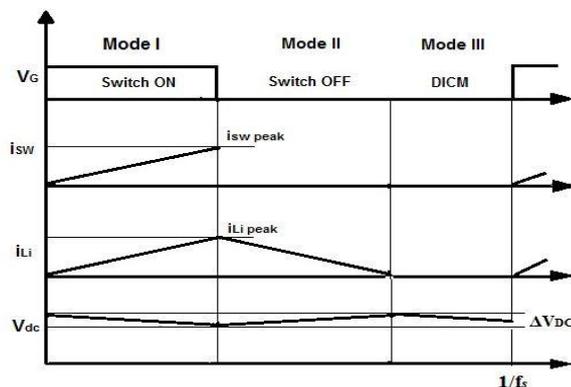

Fig 2(f)

Fig 2(g)- waveforms during switching cycle

IV. DESIGN OF CONVERTER, INPUT FILTERS AND INVERTER SELECTION

A PFC BL buck–boost converter is intended to work in DCM such that the current in inductors Li1 and Li2 will be discontinuous in a switching period. A converter is designed for power (Po =350W). The average voltage appearing at the input side for a supply voltage with an rms value of 220 V, is given as

$$V_{in} = \frac{2*1.414*V_s}{\pi} = \frac{2*1.414*220}{\pi} = 198V$$

The duty ratio (d) of the buck-boost converter calculated by the formula

$$d = \frac{V_{dc}}{V_{dc} + V_{in}}$$

The converter is designed for minimum DC link voltage of 50V (V_{dc} min) to 200V (V_{dc} max) with nominal value of 100V. The corresponding duty cycle varies from 0.2016 to 0.5025.

DESIGN OF INPUT INDUCTORS (L_{i1} & L_{i2}):

The value of the inductors to be operated in critical conduction mode can be calculated by using formula

$$L_{ic} = \frac{R(1-d)^2}{2*f_s}$$

R is the equivalent load resistance, f_s is the switching frequency. The power corresponding to minimum duty ratio and minimum dc link voltage (50V) is 90W. Hence Lic1 can be written as

$$L_{ic} = 442.67\mu H$$

In order to ensure the converter to be operated in DCM mode the values of Inductances L_{i1} & L_{i2} are take the values L_{i1} & L_{i2} are taken as 60µH. This reduces the size, cost as well as weight of the power converter.

DESIGN OF DC LINK CAPACITOR (C_d):

The DC link capacitor is design mainly depends on amount of second-order harmonic current flowing through it. The supply current (i_s) should be in phase with supply voltage (V_s) for PFC operation. Hence input power is given by

$$Pin = \left(\sqrt{2} * V_s * \sin wt\right) * \left(\sqrt{2} * I_s * \sin wt\right)$$
$$= V_s I_s (1 - \cos 2wt)$$

Here second term corresponds to 2nd harmonic reflected in dc link capacitor. Hence

$$ic(t) = -\frac{V_s * I_s}{V_{dc}} \cos 2wt$$

The ripple DC voltage corresponding to this capacitor current is given by

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$$\Delta V_{dc} = \frac{1}{C_d} \int i_c(t).dt = -\frac{I_d}{2wC_d}\sin 2wt$$

The maximum voltage ripple at dc link voltage is obtained when sin wt=1, hence above term is rewritten as

$$C_d = \frac{I_d}{2w\Delta V_{dc}}$$

Hence the value of the capacitor is calculated with allowable voltage ripple of 3%.
Hence,

$$C_d = \frac{I_d}{2w\Delta V_{dc}} = \frac{\frac{P_o}{V_{dc\,des}}}{2w\Delta V_{dc}} = \frac{\frac{350}{100}}{2*314*0.03*100}$$

$$= 1857.7\mu F$$

Hence value of C_d is taken to nearest value 2200μF

DESIGN OF INPUT FILTERS (L_f & C_f):

In order to absorb the higher order harmonics a second-order low-pass LC filter is used at the front end of the converter. Hence value of filter capacitor is calculated as[10]

$$C_{max} = \frac{I_{peak}}{wL * V_{peak}}\tan\theta$$
$$= \frac{350}{220}*\frac{1}{314*220*\sqrt{2}}\tan 1^o = 401.98nF$$

Here I_{peak}, V_{peak}, wL, and θ represent the peak value of supply current, supply voltage, line frequency in rad/sec, and displacement angle between the supply voltage and supply current, respectively.
Hence value of C_f is chosen as 330nF. The value of filter inductor (L_f) is calculated by considering source impedance (L_s) of 4%-5% of base impedance. The required inductance is calculated as[12]

$$L_{req} = L_f - L_s$$
$$L_{req} = \frac{1}{4\pi^2 f_c^2 C_f} - 0.04\frac{1}{314}\frac{220^2}{350}$$

$$= 1.57mH$$

Hence the inductance of 2.6mH is selected inorder to reduce harmonics.

V. CONTROL OF PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

CONTROL OF PFC CONVERTER:
A simple voltage follower approach helps in control of PFC converter operated in DCM mode at the front end. PWM pulses are generated by comparing DC link voltage and the reference voltage and is given to switches S_{w1} & S_{w2}. The reference voltage ($V_{dc}*$) is generated as

$$V_{dc}* = k_v\,w*$$

Where k_v and $w*$ are the motors voltage constant and reference speed.

The error voltage generated by comparing $V_{dc}*$ and DC link voltage (V_{dc}) is given to Proportional-integral (PI) controller to generate controlled output voltage Vcc. Finally the output voltage (V_{cc}) is compared with high frequency saw-tooth wave (m_d) to generate PWM pulses as

For $V_s > 0$;
$$\text{If } m_d < V_{cc}, \text{ then } S_{w1}= ON$$
$$m_d \geq V_{cc}, \text{ then } S_{w1}= OFF$$

For $V_s < 0$;
$$\text{If } m_d < V_{cc}, \text{ then } S_{w2}= ON$$
$$m_d \geq V_{cc}, \text{ then } S_{w2}= OFF$$
S_{w1} and S_{w2} are the switching signals.

COMMUTATION OF BLDC MOTOR:
The proper switching of VSI ensures that symmetrical current is drawn from the DC link capacitor for 120 degree.
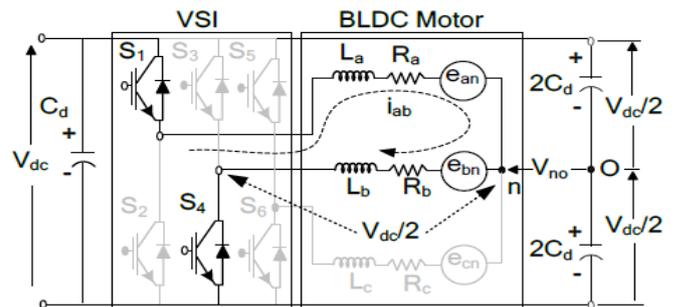

Fig 3(a)-Operation Of VSI-fed BLDC motor

Hall sensors are used in order to sense the rotor position. For every 60 electrical degrees of rotation, one of the Hall sensors changes the state. Hence the switching states for achieving electronic commutation of BLDC motor based on hall signal is given as below in table.

$\theta\,(^o)$	Hall Signals			Switching States					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

Fig 3(b)- Commutation sequence

VI. SIMULATION OF PROPOSED CONVERTER

The performance of the drive is simulated in PSIM environment and the parameters such as supply voltage (Vs), supply current (*is*), DC link voltage (Vdc), inductor currents (IL1 & IL2), switch currents & switch voltage are analyzed to demonstrate its proper functioning. Also the power factor and total harmonic distortion (THD) are analyzed to determine power quality at AC mains.
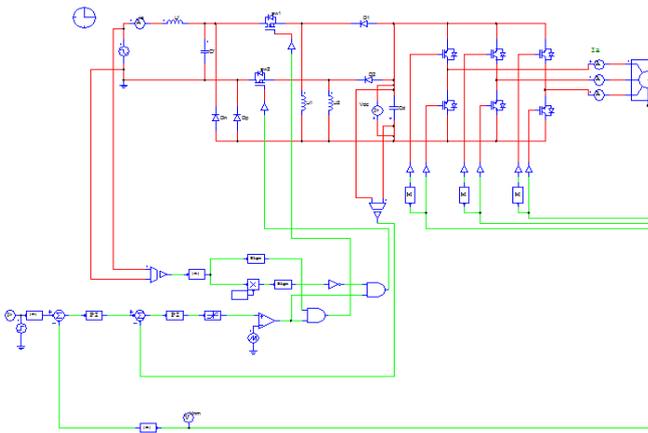
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Fig 4 (a) - Simulation circuit

The simulation results are as shown below
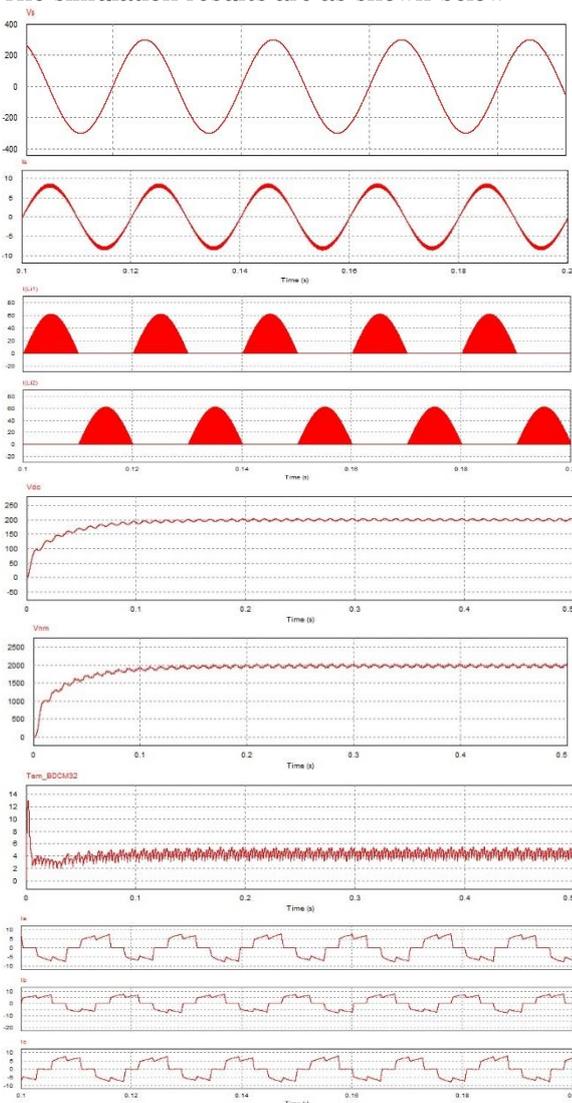

Fig 4(b) - Waveforms

The plot of supply voltage (V_s), supply current (I_s), Inductors currents (I_{L1} & I_{L2}), DC link voltage (V_{dc}), speed (rpm), Torque (Nm) and Phase currents (Ia, Ib, Ic) are shown in Fig 4(b).

Further various circuits are analyzed by connecting various loads such as constant speed, mechanical load (resistive) and linear voltage change applications etc.

CONCLUSION

This paper presents the simulation of closed loop speed control of Bridgeless PFC Buck-Boost converter feeding BLDC motor. When BLDC motor is fed by DBR, it results in PF below 0.5.Hence the PF can be improved at the AC mains by this converter. THD can be reduced to the order of 3.55% which are below the limits set by international electrotechincal standards (IEC 61000-3-2 phase), by using a low pass filter at the input side, the PF can be increased upto 0.9978. The circuit is also analyzed for mechanical loads in the PSIM environment. The hardware development of prototype is planned to validate the performance of converter.

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