Design of biquad universal filters using BD-DDCC
Chandan kumar choubey\textsuperscript{1}, Nachiket Raju Hedao\textsuperscript{2}, and Sneha balu Shedge\textsuperscript{3}

\textsuperscript{1,2,3}Dr. D. Y. Patil School of Engineering, Department of E&TC, Charholi, Pune
\textsuperscript{1}Chandan.ism@rediffmail.com, \textsuperscript{2}nachiket.22feb@gmail.com
\textsuperscript{3}snehashedge5@gmail.com

Abstract: Enhancing the performance of analog circuits with sub-volt supplies becomes a great challenge for designers. This paper presents an ultra-low voltage CMOS topology for DDCC based on the Bulk Driven (BD) principle to design a universal bi-quadratic filter performing five simultaneous standard functions: All pass, band pass, low pass, band reject & high pass. The proposed circuit employs 2 BD-DDCC and minimum grounded passive elements. The performance of the proposed circuit is confirmed from PSPICE simulation results using the TSMC 0.18um CMOS technology to prove the functionality.

Keywords: - DDCC, filter, bulk driven (BD), CMOS.

I. INTRODUCTION

In modern electronics, designs use low power analog signal processing and low voltage supply\textsuperscript{[1]-[3]} to reduce the cost, size and weight of portable devices. Over the last few years, many techniques have been introduced in analog electronics literature. Some of these techniques are quasi-floating-gate (QFG) bulk-driven (BD), floating-gate (FG), and other structures\textsuperscript{[3-7]}. The BD principle was first presented in 1987\textsuperscript{[10]}. Based on this principle, many interesting LV active building blocks were designed. In recent years, BD technique has attracted strong interest from researchers. In this paper, a new bulk driven based DDCC is proposed to obtain flexibility in analog IC design. The proposed Bulk driven based DDCC is used in a biquad in order to show the versatility of the this block. The BD-DDCC circuit and biquad are simulated with SPICE simulation Software by using 0.18 \mu m technology parameters. Simulation results show that the proposed circuit building block can be used to design filters with linearly tunable characteristics.

II DDCC

The differential difference current conveyor (DDCC) was introduced in 1996 \textsuperscript{[8]}. It combines the good features of a differential difference amplifier (DDA), like low output impedance, high input impedance, low number of components, and capability of performing arithmetic operations, and the advantages of a current conveyor (CCII), such as bandwidth, accuracy and high gain\textsuperscript{[8]}. Therefore, the DDCC has been utilized in many interesting applications \textsuperscript{[11, 12, 13, 16-18]}. The DDCC has 3 voltage terminals namely \(V_{y1}, V_{y2}\) and \(V_{y3}\) which acts as a high input impedance and \(X\) terminal is low output current impedance terminal. Thus if realization connected between output terminal \(X\) and any input terminal \(Y\), it will be acts as a low output impedance and high-input impedance.

The characteristics of DDCC is described in matrix relation is shown below:

\[
\begin{bmatrix}
i_{y1} \\
i_{y2} \\
i_{y3} \\
v_{x} \\
i_{z}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & -1 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0
\end{bmatrix} \begin{bmatrix}
v_{y1} \\
v_{y2} \\
v_{y3} \\
i_{x} \\
i_{z}
\end{bmatrix}
\]

The circuit structure of the active block as introduced. The bulk driven based DDCC is shown in Fig 2

- Transistors M7, M8, M9, M10 and M13 act as a current mirror in which applying the constant current source \(I_{bias} = 5\mu A\).
- It consists of 2 Bulk Driven differential input stages M3, M4 and M1, M2.
- Transistors M7 and M8 are common for both Bulk driven differential input stages.
The proposed biquad circuit configuration is shown in Fig. It consists of 2 DDCC's and 4 passive elements (2 capacitors and 2 resistors).

### III PROPOSED CIRCUIT

The proposed biquad circuit consists of 2 DDCC's and 4 passive elements (2 capacitors and 2 resistors). The following transfer function:

\[
V_{\text{out}} = \frac{S^4 C_1 C_2 V_{\text{in}2} + S^2 C_2 V_{\text{in}2} + V_{\text{in}1}}{S^4(C_1 C_2) + S^2 \left(\frac{C_2}{R_1}\right) + \frac{1}{R_1 R_2}}
\]

The following transfer function:

\[
V_{\text{out}} = \frac{S^4 C_1 C_2 V_{\text{in}2} + S^2 C_2 V_{\text{in}2} + V_{\text{in}1}}{S^4(C_1 C_2) + S^2 \left(\frac{C_2}{R_1}\right) + \frac{1}{R_1 R_2}}
\]

Its is clearly seen from above equations:

- The all pass response can be obtained when \( V_{\text{in}1} = V_{\text{in}2} = 0 \) (grounded) and \( V_{\text{in}3} = 1 \) and \( V_{\text{out}} \) is output.
- The band reject response can be obtained when \( V_{\text{in}1} = V_{\text{in}2} = 1 \) and \( V_{\text{in}3} = 0 \) (grounded) and \( V_{\text{out}} \) is output.
- The high pass response can be obtained when \( V_{\text{in}1} = V_{\text{in}3} = 0 \) (grounded) and \( V_{\text{in}2} = 1 \) and \( V_{\text{out}} \) is output.

### IV SIMULATION AND RESULTS

The proposed bd-ddcc was simulated by using SPICE model 0.18 μm TSMC CMOS technology parameter. This technology is used for the NMOS and the PMOS transistors. The aspect ratios of the MOS transistors, occurred in the bd-ddcc implementation, are illustrated in Table I.

The supply voltage \( V_{DD} = 0.3V \), \( V_{SS} = -0.3V \) and \( I_{\text{BIAS}} = 5μA \). The value of the capacitances \( C_1 = 2nF \) and \( C_2 = 2nF \) and resistances \( R_1 = R_2 = 10K\Omega \). These values are designed to obtain AP, BP, LP, BR and HP filters. For the proposed BD-DCDDC output displays the port relationships of ports with respect to \( V_X \).

The DC curves \( V_X \) versus \( V_{V1} \) is shown in Fig. 4. In this response \( V_{V2} \) and \( V_{V3} \) are connected to ground and \( V_{V1} \) is varied from -350mV to 350mV. The output \( X \) also varies the input \( V_{V1} \) but at certain voltage (250mV) it can diverged. The DC curves \( V_X \) versus \( V_{V2} \) is shown in Fig. 6. In this response input varies from -350 to 350mVs and \( V_{V1} \) is varied from -350 to 350mVs the same as the \( V_X \). The frequency responses of the voltage gains \( V_X/V_{V1} \) and \( V_X/V_{V2} \) is shown in Fig. 5. The current gain and low frequency voltage are equal to 1 and their -3dB bandwidth is 42MHz. The DC curve \( I_X \) versus \( I_Z \) is shown in Fig. 7. Here \( I_Z \) follows the input \( I_X \) but after 5μAmp (biasing current). The frequency response of current gain \( I_Z/I_X \) is shown in Fig. 8 and its -3dB bandwidth is 596KHz.

### TABLE I: Transistors aspect ratios and component values

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W(μm)</th>
<th>L(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, M2, M3, M4</td>
<td>100</td>
<td>0.3</td>
</tr>
<tr>
<td>M5, M6</td>
<td>50</td>
<td>0.3</td>
</tr>
<tr>
<td>M7, M8, M13</td>
<td>4</td>
<td>0.3</td>
</tr>
<tr>
<td>M9, M10</td>
<td>8</td>
<td>0.3</td>
</tr>
<tr>
<td>M11, M12</td>
<td>100</td>
<td>0.3</td>
</tr>
<tr>
<td>M9C, M10C</td>
<td>50</td>
<td>2</td>
</tr>
<tr>
<td>M11C, M12C</td>
<td>100</td>
<td>2</td>
</tr>
</tbody>
</table>
The simulated results for the AP, LP, BP, BR and HP filters characteristics are shown below fig. 9. The frequency at which all these filters are worked properly is 10 KHz which is shown in fig 9. The frequency response of phase and gain of all pass filter is shown in fig 10. The input and output response of band pass filter for 1KHz is shown in fig. 11.
1.0ms

fig:11 The input and output response of BP filter

CONCLUSIONS

In this paper, a new approach called differential difference current conveyor for realizing filters applications has been presented. Simulation results done by PSPICE confirm the validity of the theory and demonstrate the use of the DDCC.

REFERENCES


