# NoC Design Space Exploration using BAT Algorithm: An Energy-Aware Approach

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**Abstract** — Network-on-Chip (NoC) has been introduced as a solution to the communication problems for on-chip multi-processors systems. In order to minimize the energy requirement of NoC, an efficient mapping method and switch architectures are important. This research focuses on application task mapping onto NoC architecture using BAT algorithm. This paper considered Many--to--Many mapping between switches and IP cores instead of one-one mapping. The proposed method was evaluated by controlled simulation and found 10-20% energy saving compared to contemporary methods.

**Index Terms** —Network-on-Chip, Many-Many Mapping, BAT Algorithm, Design Space Exploration

## I. Introduction

As technology scales and chip density grows, on-chip communication infrastructure is playing an crucial role in System-on-Chip (SoC) communication design [1-3]. The NoC architecture consists of a grid of nodes and switches, where each node (IP, DSP, etc) connect to other nodes via switches. The mapping problem of IPs' onto NoC infrastructures has been address by many authors in the past. J. Hu and R. Marculescu presented the mapping IP cores on mesh-based NoC architectures using branch and bound approach to minimize the power consumption [4-5]. K. Srinivasan and K. S. Chatha [6] proposed a Genetic Algorithm based technique to maps the communication traces onto NoC. The objective was to minimize the power consumption and chip area. Guz, Z., Walter, I., and Bolotin, E. [7] proposed a model to minimize the bandwidth and energy consumption for the wormhole NoC having non-uniform link bandwidth. However, this method was tested using each link bandwidth customizing for a specific application after the tasks of the application are scheduled onto NoC. Therefore this model cannot be generalized and used as the mapping step of NoC design. On the other hand, NoC mapping is a quadratic assignment problem. It is difficult to find an optimal solution in time. Genetic Algorithm (GA) is a good candidate for this type of problem; however GA will make some useless iteration in later period because of the underutilization of the feedback information. So, best near optimal solutions are very hard to achieve. So, BAT Algorithm [8] can be applied to get more qualitative results.

In this paper:

- A switch model, which can connect to the core in many-many fashion instead of one-one connection.
- A BAT [8] based algorithm to map the application tasks onto NoC backbone such that the consumption of NoC based system is minimized.

The remaining part of this paper is organized as follow: In Section 2 give the overview of NoC platform characterization, which is a very important part of this approach. Section 3 outlines the working principle BAT algorithm. Section 4 discussed the details of the proposed design space exploration. The experimental results in Section 5 show the benefit of using our mapping algorithm. Finally, we summarize this work in Section 6.

## II. NoC platform characterization

The most important aspects of the methodology are the characterization of NoC platform and the formulation of mapping algorithm. So, this section briefly discusses the characteristics of our NoC platform, which is very crucial to formulate the NoC mapping problem. The mapping between switch and Core(tile) is very important for the performance of the NoC system. The Figure 1 shows how can a core(tile) can be bind to adjacent switches. This (many-many) type of binding drastically reduced the congestion in the network by uniformly distributing the load in different channels and also reduced the total energy consumption. Sub-section below discusses about the switch design for many-many binding.

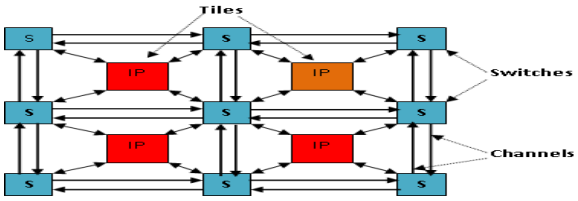


**Figure 1**: Many-many mapping NoC architecture *A Switch design*

In this research mesh based NoC architecture for the design space exploration problem was considered. The structure of the switch with storage buffers is shown in the Figure 2. It also shows, the connection between cores and switches using many-many mapping i.e a core can connect at most '4' switches and a switch can connect at most '4' cores [3].

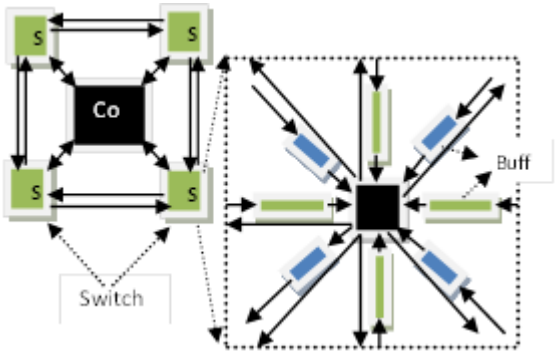


**Figure 2:** Core-Switch binding and Switch structure

### *B. NoC Platform*

*NoC Topology:*

Finding a suitable NoC topology for a NoC design is a crucial task. There are many topologies are available e.g mesh, torus, cube, fat tree and butterfly, etc. in the literature [9] and are often used in NoC design. In this paper, a regular topology called 2D-mesh is used as NoC platform for its simple structure.

*Switching Technique:*

Several switching techniques (e.g., store-and-forward, virtual-cut-through, wormhole and circuit switching) are being used in NoC design space exploration problems considering merit and demerit in different situation and applications. Considering the resources limitation in NoC, wormhole routing technique was used in this research.

*Routing technique:*

Routing algorithms are also played a crucial role in NoC design. NoC routing techniques can be classified into two groups i.e deterministic and adaptive routing. In this research deterministic routing algorithm without deadlock (e.g., XY routing algorithm [10]) was used.

## III. Bat Algorithm

BAT algorithm (BA) is derived from Darwin's evolution theory. Both of them use the common steps of evolution such as selecting the best individuals, updating the population according to environmental changes and elimination of weak individuals to increase the survival rate of populations. BAT algorithm is first proposed by Yang [8] with the adaptation echolocation behaviour of bats. Bats are quite good in navigation even in the darkness by using their well-developed system called echolocation. They send echo to the objects and from the reflection of that echo, distances, coordinates and even the identification of objects can be determined. The bat algorithm uses this powerful echolocation behaviour of bats. According to BA, each bat in the population moves towards to prey with a velocity ($V_i$) at position ($X_i$) with frequency (f), rate (r) and loudness (A). In each iteration, the values are updated for each bat who moves to the prey, until a bat reached to the food source. The steps of BA is given below.

*BAT Algorithm*

Step 1. Initialize the population of bat with variables; velocity (V), position (X), frequency (f), rate (r) and loudness (A).

Step 2. Calculate the fitness value of each bat and rank them.

Step 3. Update the variables V, X, f, r, and A by applying following equations;

$f_i = f_{min} + (f_{max} - f_{min})\beta$ ----------(1)

$V_i^{t+1} = V_i^t + (X_i^t - \text{Best})\, f_i$----------(2)

$X_i^{t+1} = X_i^t + V_i^{t+1}$ ---------- (3)

$A_i^{t+1} = \propto A_i^t$ ---------- (4)

$r_i^{t+1} = r_i^0[1 - exp^{\gamma t}$---------- ---------- (5)

Step 4. If (rand $> r_i$)

Select a solution among the best ones.

Generate a solution around the selected solution by using the following equation;

$X_{new} = X_{old} + \varepsilon A_i^t$ ---------- (6)

else

Generate a new solution randomly.

Step 5. If (rand$< A_i^t$ & $f(X_i) < f(X_i^*)$)

Accept new solution to the population

Step 6. Calculate the fitness value of each bat.

Step 7. Repeat steps 3-6 until a stopping criterion is met

β is a random number in between (0-1), $f_{max}$ and $f_{min}$ are the boundaries of frequency (0-100), Best is the best solution achieved so far by the algorithm in the population, α and $\gamma$ are the constants to update the loudness (A) and rate (r) in between (0-1), ε is a random number in between (0-1), At is the average loudness at time t.

## IV. Design Space Exploration Methodology

Figure -3 summarized the proposed design space exploration framework. The Task applications are represented using a task graph in the proposed framework [3]. The task graph (Core Communication Graph (CCG)) is presented as a directed graph $G$ (Vertex(V), Edge(E)). Each vertex $v_i \in V$, representing a task and the directed edge $< v_i, v_j >$, denoted as $e_{ij} \in E$ , representing the communication dependency between the cores $v_i$ and $v_j$ . Each edge ($e_{ij}$) has associated with two values ($V_{ij}$ and $D_{ij}$). Where $V_{ij}$ represents the required bandwidth and $D_{ij}$ represents delay. Another constraint (d) is associated with task graph, which represent the execution deadline of the task graph [3].

The NoC architecture of the proposed framework is represented by the NoC topology graph (Architecture Characterization Graph (ACG)). The NoC topology graph is presented as a Directed Graph Ĝ(Tile(T), Route($\mathfrak{R}$) ).Where, each vertex $t_i \in$ T, representing a tile (node) in the topology and the directed edge $< t_i, t_j >$, denoted as , $r_{ij} \in \mathfrak{R}_s$ representing a directed communication between the vertices $t_i$ and $t_j$ . The weight of each edge ($r_{ij}$) is denoted by the order pair$< d_{ij}, b_{ij} >$, where $d_{ij}$ represents the delay and $b_{ij}$ represents the maximum allowed bandwidth of the communication from $t_i$ to $t_j$[3].

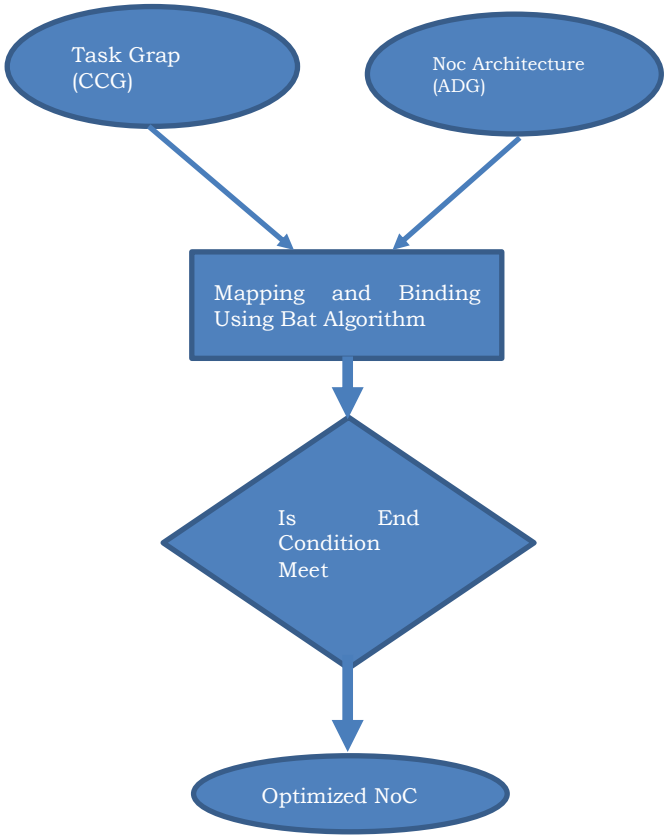


**Figure 3**: Outline of design space exploration framework flow

In the proposed methodology, the core communication graph (CCG) and the architecture characterization graph (ACG) is given as an input[3].

Then BAT Algorithm (BA) based techniques has used to explore the design space. There are two important tasks in the whole design space exploration i.e mapping and binding. In the mapping phase, first the tasks in CCG are order based on their communication volume ($v_{ij}$) and then mapped to the IPs in the ACG using BA. In the second phase, many-many binding between IPs and the switches is performed as shows in Figure 3.

The dimension of the NoC architectures are decided accordingly to the sizes of the task graph in the proposed framework. If the size of the architecture is not chosen properly, it may lead to significant area overhead. Therefore it is very important to choose a proper size of the architecture, since it may lead to significant area overhead if the size of determining the proper dimensions of the architecture is very crucial for the design space exploration. In order to map all the functioning blocks into the NoC architecture, the following condition should be satisfied. i.e *Total number of vertices (|V|) in the task graph ≤ Total number of vertices (|T|) in the NoC architecture characterization graph.* After obtaining the specification for CCG and ACG, mapping of the task graph onto the topology graph is the next step in the proposed framework flow.

*A. Objective Function*

The main objective of this paper is the energy consumption. So, energy consumption is defined as follows: The energy $E_{bit}^{p(t_{v_i},t_{v_j})}$ that every bit consume while route through $P\left(t_{v_i},t_{v_j}\right)$ :

$$E_{bit}^{p(t_{v_i},t_{v_j})} = (|p(t_{v_i},t_{v_j})|+1)\times E_R + |p(t_{v_i},t_{v_j})|\times E_L \quad (7)$$

Where $P(t_{v_i},t_{v_j})$ indicate the set of routing paths (P) that connect core $v_i$ onto tile i to core $v_j$ onto tile j. It is a set of several links {$l_j$, $l_{j+1}$, . . . }. Where $|P(t_{v_i},t_{v_j})|$ is the hop of path $P(t_{v_i},t_{v_j})$, and $E_R$ is the energy consumed by a router, $E_L$ is the energy consumed by a link.

Then the energy $E_{e_{ij}}$ that a communication edge routes though the path $P(t_{v_i},t_{v_j})$ :

$$E_{e_{i,j}} = v(e_{i,j})\times\{(|p(t_{v_i},t_{v_j})|+1)\times E_R + |p(t_{v_i},t_{v_j})|\times E_L\} \quad (8)$$

The total energy requirement is denoted by $E_{E_C}$, which represents the sum of links' energy and IP energy:

$$E_{E_C} = \sum_{e_{i,j}\in E_C} v(e_{i,j})\times\{(|p(t_{v_i},t_{v_j})|+1)\times E_R + (|p(t_{v_i},t_{v_j})|)\times E_L\} \quad (9)$$

*B. Mapping Algorithm*

In our approach, a mapping algorithm that minimized the requirement of energy consumption is explored. Our exploration unveils BAT Algorithm (BA) in finding the best solution because NoC mapping is a QAP (Quadratic Assignment Problem) [14]. BA inspired by Darwin's evolution theory is a probabilistic optimization technique, which is often used to solve the NP (Non-deterministic Polynomial) problem.

The problem of energy minimizing can be formulated as follows:

**Given:**

1) Core Communication Graph, ***G*** (V, E)

2) NoC Architecture Characterization Graph Ĝ( T, $\mathfrak{R}$ ).

3) Routing algorithm (**$\check{R}$**)

**Determine:**

I. A mapping from the set of tasks *T* to the set of processors *P*

II. Many-many binding between tiles and switches

**Such that:**

The total Energy $E_{E_C}$ is minimized, i.e. Min ($E_{E_C}$) *s.t. G (V, E)* , Ĝ( T, $\mathfrak{R}$ ), $\check{R}$

## V. Experimental Results

In order to evaluate the benefit of using the mapping algorithm proposed in this paper, a cycle-accurate mesh NoC platform in C++ level is constructed. The XY routing, which first routes packet along the X-axis until the packets reach the column where lies the destination tile and then routes packet along the Y-axis, is used. The packets which consist of 32 flits and each flit has 16 bit are used in our experiments. Various experiments are conducted to verify the efficiency of the proposed algorithm. GA and PSO based approaches are considered for comparison with proposed BA. All of the algorithms are compiled by C++ and run on Windows XP in a computer with Intel P IV 3.4GHz CPU and 2GB memory. In 0.18µm technology, it is assumed that the link length is 2mm, the total line capacitance is 0.5fF/µm and voltage swing is 3.3v, then $E_L$ is 5.445pJ and $E_R$ is 0.43pJ [15].

### A. Randomly Generated Applications

All random tasks are generated by TGFF [16].Table I shows the detail of each task, including number of IP cores, number of directed arcs, total communication volume and NoC Size.

**Table 1**: Randomly generated Task

| Task no. | No. of IPs | No. of directed edge | Total volume of communication |
|---|---|---|---|
| 1 | 9 | 12 | 1186 |
| 2 | 16 | 24 | 1980 |
| 3 | 16 | 20 | 1672 |
| 4 | 25 | 37 | 12456 |
| 5 | 35 | 46 | 11832 |

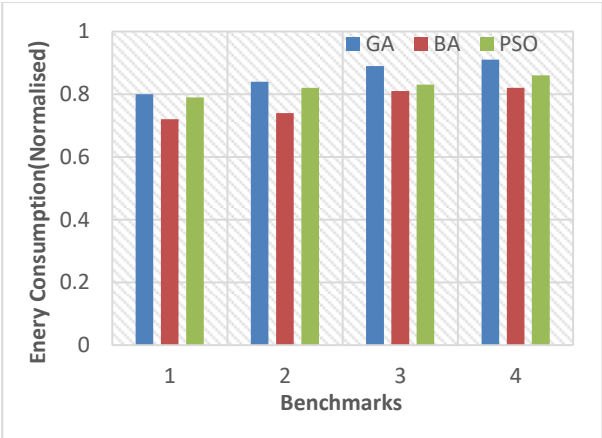


Figure 4: Energy consumption result

Experimental result shows that the energy consumption is minimized using our proposed approach in compare to random mapping and mapping using GA. The result from the Figure 4 shows that on an average our approach reduce the energy consumption around 40% in compare to random mapping and around 20-25% in compare to GA. The time taken for each algorithm is shown in the Table-2.

Table-2: Time Comparative results

| Task no | GA | PSO | BA |
|---|---|---|---|
| 1 | 1.7s | 9s | 1.6s |
| 2 | 3.9s | 13.7s | 4.1s |
| 3 | 3.8s | 13.2s | 3.8s |
| 4 | 6.3s | 19.2s | 6.2s |
| 5 | 7.7s | 21.2s | 7.8s |

Experimental results show that the computing time of proposed approach (BA) is less than PSO based approach and comparable to GA. Though the time difference is comparable, but the energy saving is increases with the increase of number of IP. Mapping of 35 IPs in the time difference of about 1s more could be accepted.

B. Real-world Applications

In this paper, we carried one experiment for a multi-media system (MMS) which is consisted by H.263 video encoder/decoder and MP3 audio encoder/decoder. The multi-media system can be divided into 25 IP cores. Figure 5 shows the communication volume between the IP cores.

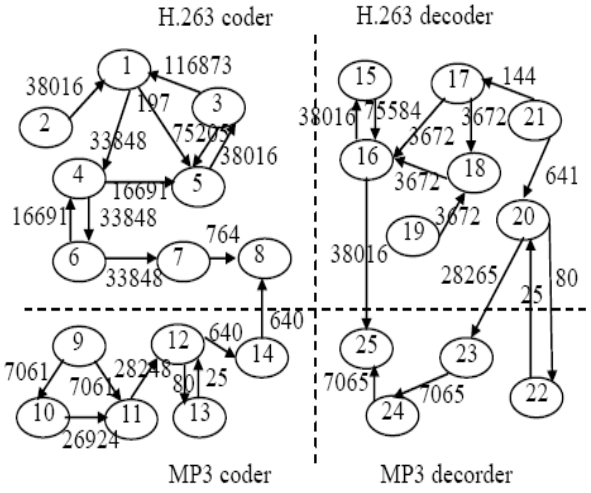


Figure 5: MMS System

Based on the above parameters, the energy consumption is calculated by proposed and other algorithm (GA) respectively as shown in Figure 6 .

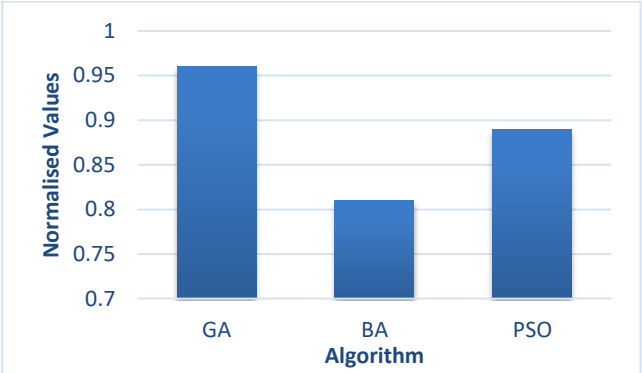


Figure 6: Energy consumption for MMS System

## Conclusion

In this paper, an efficient method to saving the energy requirement of NoC is considered. The result shows the effectiveness of the proposed method in compare to GA and PSO based mapping. Therefore, it can be used as a useful tool on NoC design to decrease NoC implementation cost.

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